United Electronic Industries

The High-Performance Alternative

DNx-AI-256

—

User Manual

2-Channel Synchro/Resolver I/O Interface
and LVDT/RVDT Simulator Interface Layer
for the PowerDNA Cube and PowerDNR RACKtangle

Release 4.5

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PN Man-DNx-AI-256-212

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Chapter 1 Introduction

This document outlines the feature-set of the DNR- and DNA-AI-256 layer and how to use it for synchro/resolver/LVDT/RVDT applications.

1.1 Organization of Manual

This AI-256 User Manual is organized as follows:

- **Introduction**
  This section provides an overview of the AI-256 common features.
- **Synchro/Resolver Input and Output/Simulator**
  This chapter provides an overview of the AI-256 synchro/resolver (S/R) interface features, device architecture, and connectivity.
- **LVDT/RVDT Simulator**
  This chapter provides an overview of the AI-256 LVDT/RVDT simulator interface features, device architecture, and connectivity.
- **Programming with the High-Level API**
  This chapter provides an overview of the how to create a session, configure the session, and format relevant data with the Framework API.
- **Programming with the Low-Level API**
  Describes low-level API commands for configuring and using the AI-256 series layer for Synchro/Resolver/LVDT/RVDT operating modes.
- **Appendix A - Accessories**
  This appendix provides a list of accessories available for use with the DNx-AI-256 Synchro/Resolver/LVDT/RVDT interface board.
- **Appendix B - Connection Diagrams**
  This appendix contains connection diagrams for various operating and synchro/resolver excitation modes of the DNx-AI-256 interface board.
- **Index**
  This is an alphabetical listing of the topics covered in this manual.

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Manual Conventions

To help you get the most out of this manual and our products, please note that we use the following conventions:

Tips are designed to highlight quick ways to get the job done or to reveal good ideas you might not discover on your own.

NOTE: Notes alert you to important information.

CAUTION! *Caution advises you of precautions to take to avoid injury, data loss, and damage to your boards or a system crash.*

Text formatted in **bold** typeface generally represents text that should be entered verbatim. For instance, it can represent a command, as in the following example: “You can instruct users how to run setup using a command such as **setup.exe**.”

Text formatted in `fixed` typeface generally represents source code or other text that should be entered verbadim into the source code, initialization, or other file.

Examples of Manual Conventions

Before plugging any I/O connector into the Cube or RACKtangle, be sure to remove power from all field wiring. Failure to do so may cause severe damage to the equipment.

Usage of Terms

Throughout this manual, the term “Cube” refers to either a PowerDNA Cube product or to a PowerDNR RACKtangle™ rack mounted system, whichever is applicable. The term DNR is a specific reference to the RACKtangle, DNA to the PowerDNA I/O Cube, and DNx to refer to both.

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1.2 The AI-256 Interface Board

The DNx-AI-256 layer is a 2-channel layer. Each channel may act as either a Synchro/Resolver input, output, or LVDT/RVDT output. It is suited for a wide variety of industrial, military, and simulator applications.

The layer is available in two versions: the DNA-AI-256 for mounting in UEI Cube products, and the DNR-AI-256 for insertion into the UEI RACKtangle and HalfRACK chassis. The DNx-AI-256 is physically a two-board module composed of one of two types of base boards (one for the DNA version and another for the DNR version) plus an AI- 256-specific daughter board. The DNA and DNR are functionally the same except for the bus connectors used. Functionally, the AI-256 is an extension of the AI-255 with higher current output and lower voltage, and also provides the LVDT/RVDT output-only functions of the AI-254 with much higher voltage and current capabilities.

The DNx-AI-256 is fully supported by the UEIDAQ Framework API, which provides a simple and complete software interface to all popular programming languages, operating systems, and data acquisition/control application packages such as LabVIEW, DASYLab, and MATLAB.

As with all UEI PowerDNA boards, the DNx-AI-256 can be operated in harsh environments and has been tested at 5*g* vibration, 50*g* shock, -40 to +85°C temperature, and altitudes up to 70,000 feet. Each board provides 350 V_{rms} Isolation between channels and also between the board and its enclosure or any other installed boards as well as electro-shock-discharge (ESD) isolation.

Software for the DNx-AI-256 is provided as part of the UEI Framework. Framework provides a comprehensive, yet easy-to-use, API that is compatible with all popular Windows programming languages and that also supports programmers using Linux and most realtime operating systems such as QNX, RTX, or RT Linux. Also, UEI Framework can be used for creating applications in LabVIEW, MATLAB/SImulink, DASYLab, or any application that supports ActiveX or OPC servers.

1.3 Features

The common features of the DNx-AI-256 are listed below:

- Two channels acting as Synchro/Resolver or LVDT/RVDT interface
- 16-bit resolution
- Signal input voltage of 5 to 28V_{rms} for Synchro/Resolver mode
- Signal output voltage up to 19.8V_{rms}
- Reference (excitation) voltage up to 19.8V_{rms} at 3.0VA in 0.6mV_{rms} increments (16-bit output resolution)
- User-programmable excitation frequency (50Hz-10kHz)
- Automatic shutdown on overload in Synchro/Resolver mode
- Isolation up to 350 V_{rms} between channel and between I/O's and GND
- Tested to withstand 5g Vibration, 50g Shock, -40 to +85°C Temperature, and Altitude up to 70,000 ft or 21'000 meters.
- Weight of 136 g or 4.79 oz for DNA-AI-256; 817 g or 28.8 oz with PPC5.
- UEI Framework Software API may be used with all popular Windows programming languages and most real time operating systems such as RT Linux, RTX, or QNX and graphical applications such as LabVIEW, MATLAB, DASYLab and any application supporting ActiveX or OPC.

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1.4 Indicators

A photo of the DNx-AI-256 unit is illustrated below.

The front panel has two LED indicators:

- RDY: indicates that the layer is receiving power and operational.
- STS: can be set by the user using the low-level framework.

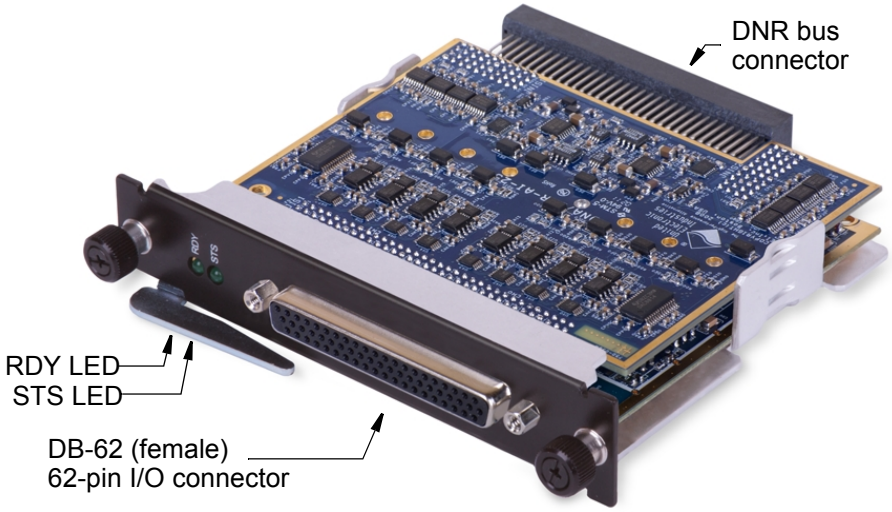

Figure 1-1. The DNR-AI-256 Analog-Input Layer

Chapter 2 Synchro/Resolver Mode

This chapter provides an overview of synchros/resolvers, how the DNx-AI-256 can be used to manipulate them, and supporting documentation to do so.

The DNx-AI-256 can act as a 2-channel *Synchro or Resolver interface* for UEI's PowerDNA and PowerDNR data acquisition systems. The board provides two channels that can monitor either 3/4-wire (plus excitation) synchros or 4-wire (plus rotor excitation) resolvers or, as an alternative, provide simulated outputs for test and simulator applications. It is capable of angle measurement accuracies approaching ±2.6 arc-minutes. Each channel may be configured either as an input or an output, in any combination. Output accuracy is ±4 arc-minutes.

The inputs may be sampled at rates up to the excitation frequency of 10 kHz. Each channel provides its own Programmable Reference Voltage with outputs independently programmable from up to 19.8 V_{rms} in increments of 0.6mV and at frequencies from 50 to 10000Hz.

The DNx-AI-256 may instead provide two channels of Synchro or Resolver Output, ideal for driving devices such as altitude indicators or as test sources for a wide range of synchro or resolver input devices. The two outputs each accept an independent reference signal and offer 16-bit output resolution. Each channel can drive up to 19.8 V_{rms} at 2.4 VA without external buffering.

2.1 Overview of Synchros & Resolvers

Synchros and resolvers are electromechanical transducers that are used either to detect and measure a rotary shaft position or to position a shaft at a desired angle. The devices can be further classified as transmitters, receivers, differentials, or control transformers.

2.1.1 The Synchro

Synchros were originally called "selsyns", for "self-synchronous". A generator and receiver are wired together so that the angular position of the generator (transmitter) shaft is automatically reproduced in the motor (receiver). Although they may appear to be similar in construction to synchronous motors and generators, the major difference between them is that the rotor of a synchro is excited with an AC voltage rather than a DC voltage. In other words, a synchro is a single phase device with AC rotor excitation and a synchronous motor or generator is typically a 3-phase (time-phase) device with DC rotor excitation.

The rotor of a synchro normally has a single-phase winding, usually referred to as a "dumbbell" rotor. The stator has 3 windings connected in a star configuration at 120°.

The AC voltage applied to the rotor winding induces AC voltages in three stator windings, which are spatially displaced 120° apart. The voltages induced in the stator windings are either in time-phase with the excitation voltage or 180° out of time-phase. The magnitudes of these voltages are:

$$V_{S1\text{-}3} = KV_{R2\text{-}1} \sin \theta$$

$$V_{S3\text{-}2} = KV_{R2\text{-}1} \sin (\theta + 120°)$$

$$V_{S2\text{-}1} = KV_{R2\text{-}1} \sin (\theta + 240°)$$

where

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θ is the rotor position angle
V_{S1-3} is the voltage between S1 and S3 terminals
V_{R2-1} is the voltage between R2 and R1 terminals
and K is the maximum coupling transformation ratio V_{out}/V_{in}

Since the set of three voltages transmitted by the synchro generator is unique for each position of the rotor throughout a 360° rotation, a synchro receiver, whose rotor is excited in parallel with the generator, measures the magnitude and time-phase relation of the voltages and produces a torque that causes the receiver rotor to move to the same angular position as the transmitter. A synchro transmitter and receiver thus form a simple synchro system.

Receiver

When the transmitter and receiver rotors are in alignment, stator voltages are equal and no current flows. If the transmitter rotor is turned (relative to the receiver rotor), a force appears in the receiver, causing the rotor to track the transmitter rotor. The torque produced is proportional to the angle difference between the two rotors. Typical accuracy of such a system is 30 arc-minutes.

A single transmitter may be parallel-connected to multiple receivers, at the cost of reducing accuracy and increasing the power drain from the source.

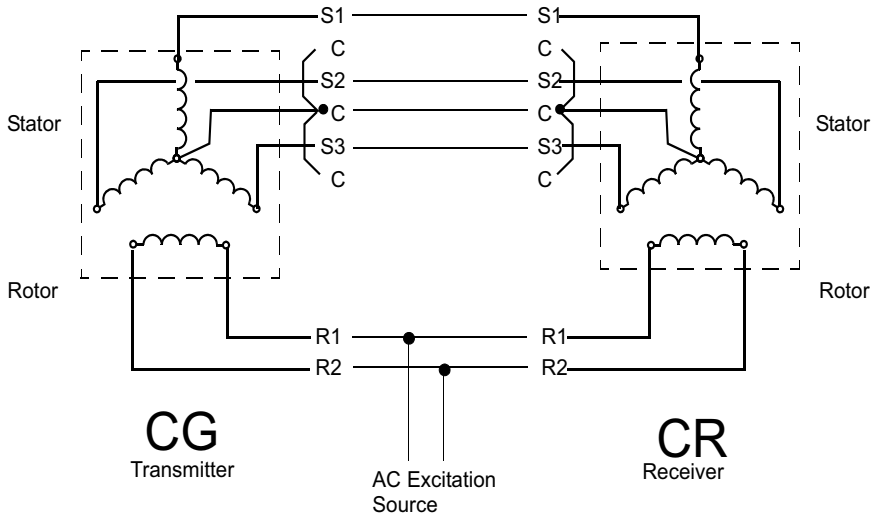

Figure 2-1. Typical Synchro Transmitter/Receiver

Control Transformer

A control transformer has a Y-connected stator and a single-phase cylindrical drum rotor. When the stator is connected to the stator of a transmitter and the transmitter rotor is turned relative to the control transformer rotor, the magnitude of the control transformer stator field remains constant, but a voltage is induced in the rotor. The magnitude of this voltage varies with the sine of the angle between the axis of the rotor and that of the stator flux. The control transformer, therefore, provides information about the transmitter rotor angular position.

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If the control transformer rotor angle differs from that of the transmitter, a voltage proportional to the sine of the angular difference appears on the control transformer rotor. This may be used as an input to a servo control system that causes the control transformer rotor to move to the same angle as the transmitter.

2.1.2 The Resolver

A resolver is a rotary transformer in which the magnitude of the energy through the resolver varies sinusoidally with rotation of the shaft. A resolver control transmitter has one primary winding (Reference Winding) and two secondary windings (the SIN and COS windings). The reference winding is located on the rotor and the SIN and COS windings are on the stator, displaced spatially by 90°. If the resolver is a brushless type, current is applied through a rotary transformer, which eliminates the problems of slip rings and brushes.

The reference winding is typically excited by an AC voltage. The induced voltages in the SIN and COS windings are equal to the reference voltage multiplied by the sine or cosine of the angle of the input shaft relative to a fixed zero position.

The connection arrangement of a brushless resolver control transformer is illustrated below in **Figure 2-2.**

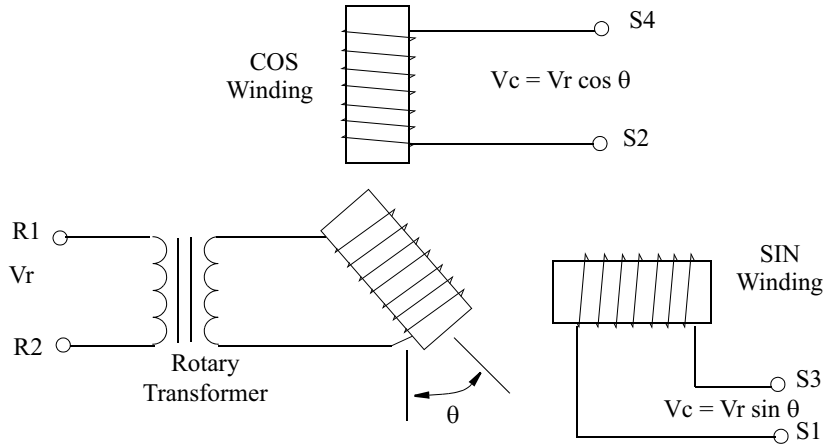

Figure 2-2. Brushless Resolver Control Transformer

2.1.2.1 Voltage Magnitude, Polarity, and Phase vs. Rotor Angle

A sine wave AC Excitation voltage $V_{exc}$is applied between R1 and R2. The voltage observed between S1 and S3 is $V_{sin} = V_{exc}$ sin A, where A is the rotor angle in radians. SImilarly, the voltage observed between S2 and S4 is $V_{cos} = V_{exc}$ cos A, where A is the rotor angle in radians. The two output voltages remain in phase with each other relative to the excitation voltage, but differ in magnitude and/or polarity (relative to excitation) as the rotor angle changes, as shown in **Figure 2-3.**

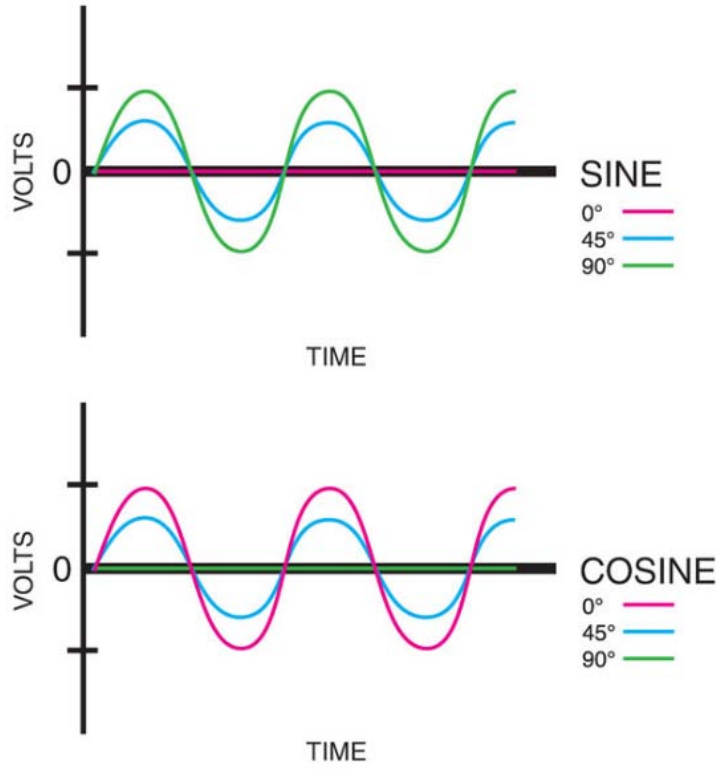

Figure 2-3. SIN and COS Output Voltages vs. Rotor Angle

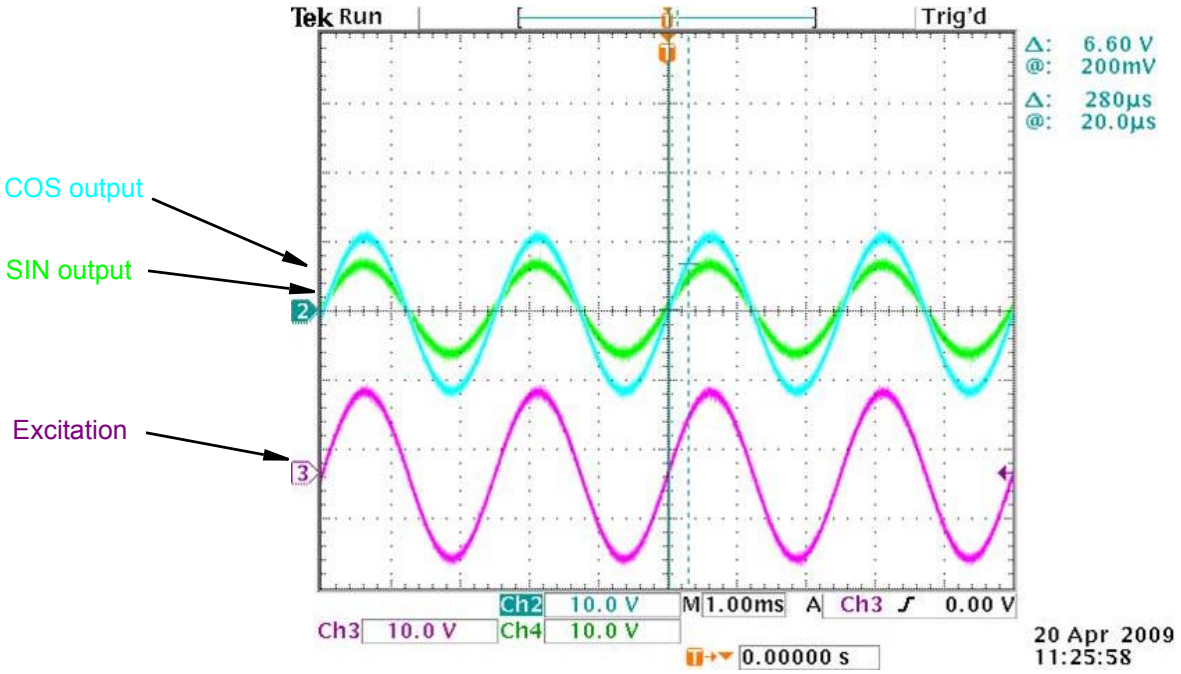

Figure 2-4. Resolver Waveforms at 30° Rotor Angle

Referring to **2-4**, The SIN and COS output voltages are in phase with excitation, have the same polarity relative to excitation, but have different magnitudes.

Referring to **2-5**, The SIN and COS output voltages are in phase with excitation, have the opposite polarity relative to excitation, but have equal magnitudes.

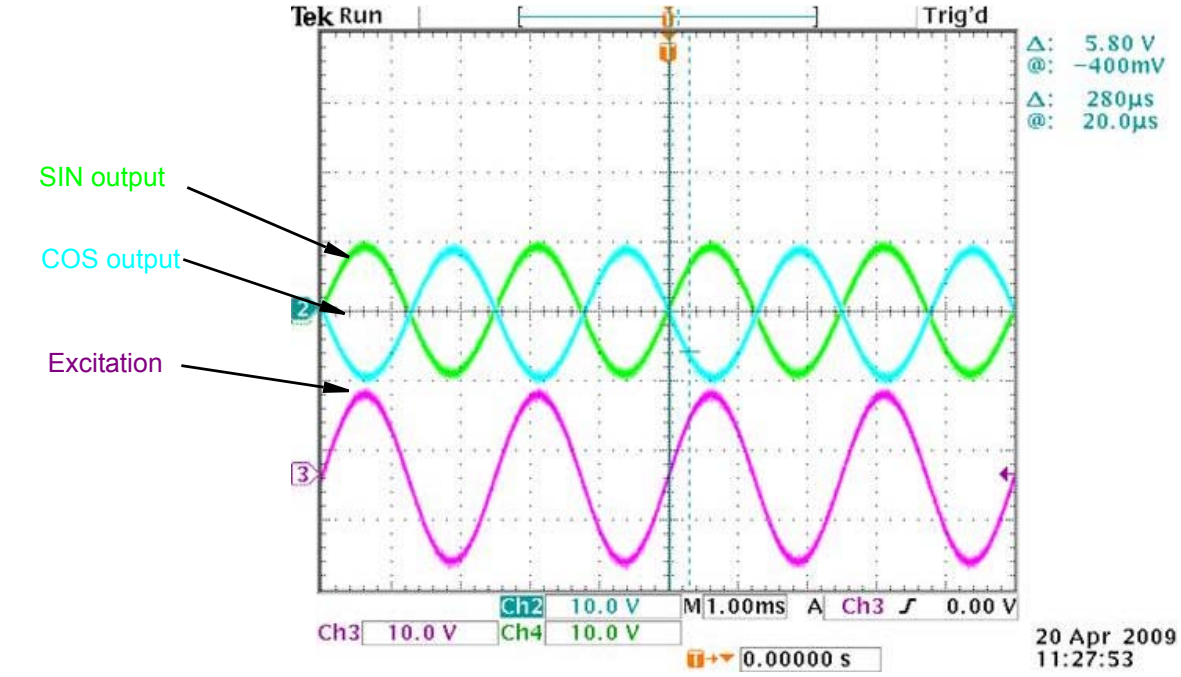

Figure 2-5. Resolver Waveforms at 135° Rotor Angle

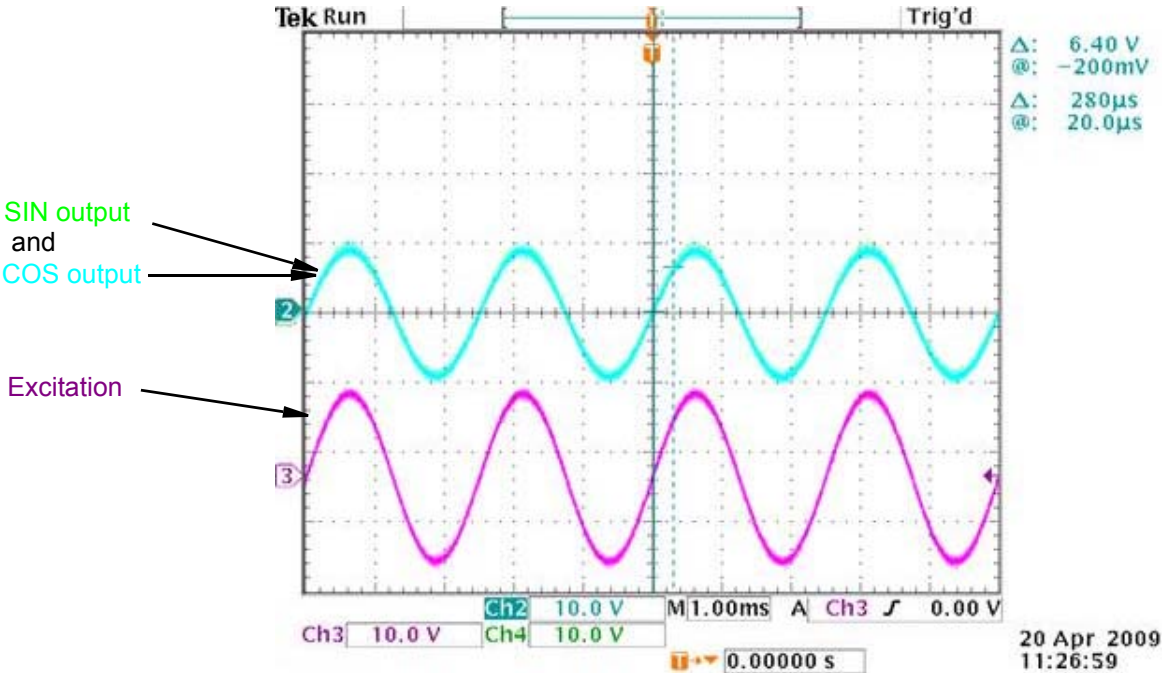

Figure 2-6. Resolver Waveforms at 45° Rotor Angle

Referring to **2-6**, The SIN and COS output voltages are in phase with excitation, have the same polarity relative to excitation, and also have equal magnitudes.

When a synchro is used, the excitation and output voltages appear as shown in **Figure 2-7.** Note that a synchro has three windings with angles between coils of 120°.

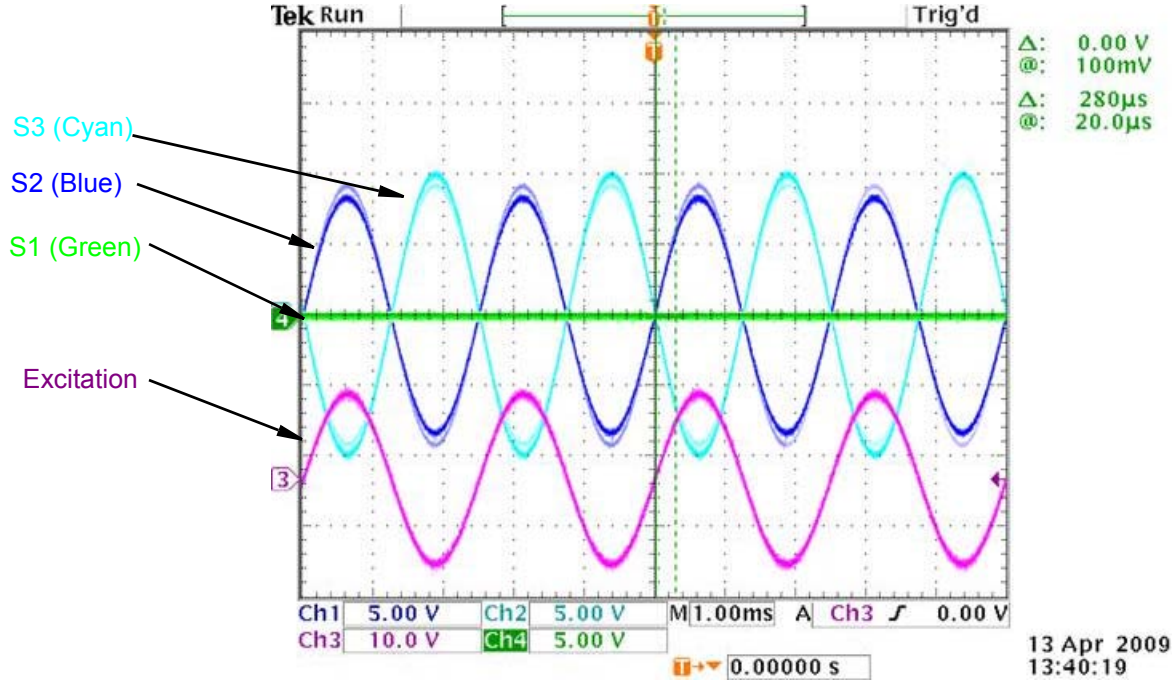

Figure 2-7. Synchro Waveforms at 0° Rotor Angle.

The SI coil output voltage (green line) is zero because the rotor is positioned plus or minus 90° relative to the S1 stator winding and therefore produces nothing. The S2 coil (blue line) shows a voltage in phase with excitation and with the same polarity as the excitation voltage. The S3 coil (cyan line) shows a voltage of polarity opposite to that of the excitation (or 180° out of phase).

NOTE: Coils on a synchro can be labeled in two different ways -- looking at the synchro from the shaft side as S1at the top, followed in a counterclockwise direction by S2 and S3, or looking at the collector side as S1 at the top, followed in a clockwise direction by S2 and S3. In datasheets from some companies, the labeling may be reversed.

NOTE: When using the AI-256 for simulation, you can attach a scope to the simulation outputs, ground the scope probes to AGND and read voltages between S1 and AGND, S2 and AGND, and S3 and AGND. Some synchros have the coil mid points between coils brought out, but most do not. To create a proper transform function, you need to consider the following formula:

$$\varphi_{actual} = 135 - \varphi_{calculated}$$

where the angle is calculated from the scope display.

Figure 2-8 below illustrates how the magnitudes of the SIN and COS output voltages vary with rotor angle. The table that follows lists the calculated data points for the graph.

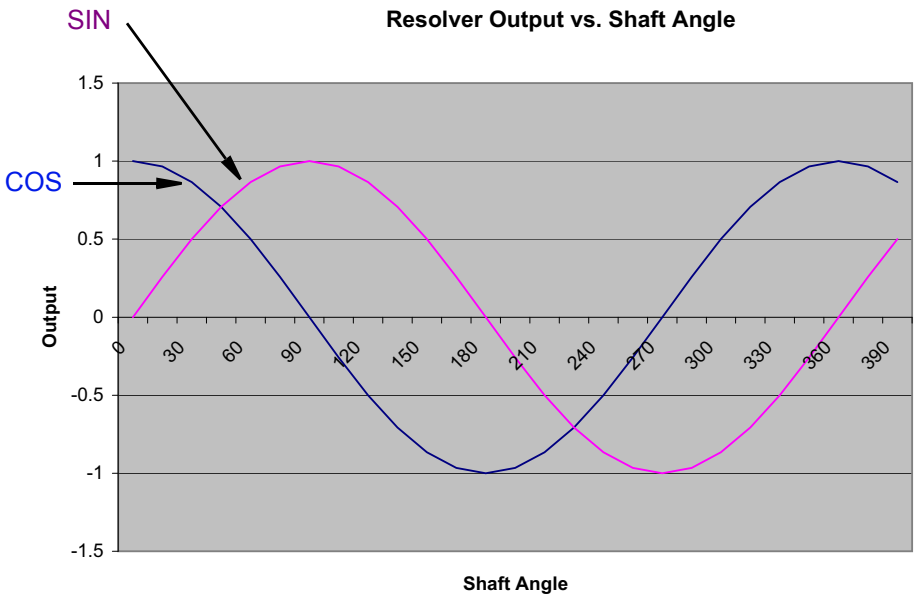

Figure 2-8. Magnitudes of SIN and COS Output RMS Voltages vs. Rotor Angle

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2.2 Specifications

Technical specifications for the DNx-AI-256 board are listed in **Table 2-1**.

Table 2-1. DNx-AI-256 Technical Specifications Synchro/Resolver

Inputs	
Number of channels	2
Configuration	Synchro (3-wire) or Resolver (4-wire) may be selected via software
Resolution	16-bit
Accuracy	± 2.6 arc-minute
Frequency	50 Hz to 10 kHz
Signal Inputs	5 - 28 Vrms
Acceleration	300 rps/s @ 60 Hz, 450 rps/s @ 400 Hz 1000 rps/s @ 4000 Hz
Step response	800 mS - 179° @ 60 Hz, 150 mS - 179° @ 2500 Hz
Update rate	Max. rate is equal to the excitation frequency.
Reference output	
Number of channels	2 (one per input channel)
Output voltage	up to19.8 Vrms at 3.0 VA (see table in specification document for other output voltages)
Voltage resolution	16 bits
Reference Frequency	50 Hz to 10 kHz (±0.1%)
Synchro / Resolver Outputs	
Number of channels	2 (total number of synchro/resolver inputs and simulated outputs is limited to 2.)
Configuration	Synchro (3-wire) or Resolver (4-wire)
Resolution	16-bit
Output Voltage	up to 19.8 Vrms up to 2.4 VA.
Output Accuracy	±4 arc-minutes
Output readback and protection	
Output protection	Automatic shut down on overload
Voltage output monitoring	±70 mV, monitored at 1.3 Hz
Current output monitoring	±1.0 mA, monitored at 1.3 Hz

Output Drive Specifications (Synchro/Resolver):

Vrms	*Vpp*	*Idcmax*	*Irms*	*VA max*	*Rlmin*
2.0	5.7	0.20	0.141	0.6	14.1
3.0	8.5	0.20	0.141	0.9	21.2
4.0	11.3	0.20	0.141	1.1	28.3
5.0	14.1	0.20	0.141	1.4	35.4
6.0	17.0	0.20	0.141	1.7	42.4
7.0	19.8	0.20	0.141	2.0	49.5
8.0	22.6	0.20	0.141	2.3	56.6
9.0	25.5	0.20	0.133	2.4	67.5
10.0	28.3	0.20	0.120	3.0	83.3
11.0	31.1	0.20	0.109	3.0	100.8
12.0	33.9	0.10	0.100	3.0	120.0
13.0	36.8	0.10	0.092	3.0	140.8
14.0	39.6	0.10	0.086	3.0	163.3
15.0	42.4	0.10	0.080	3.0	187.5
16.0	45.3	0.10	0.075	3.0	213.3
17.0	48.1	0.10	0.071	3.0	240.8
18.0	50.9	0.10	0.067	3.0	270.0

Specifications above are for a single output channel. Total output power for all channels combined may not exceed 5.0 VA

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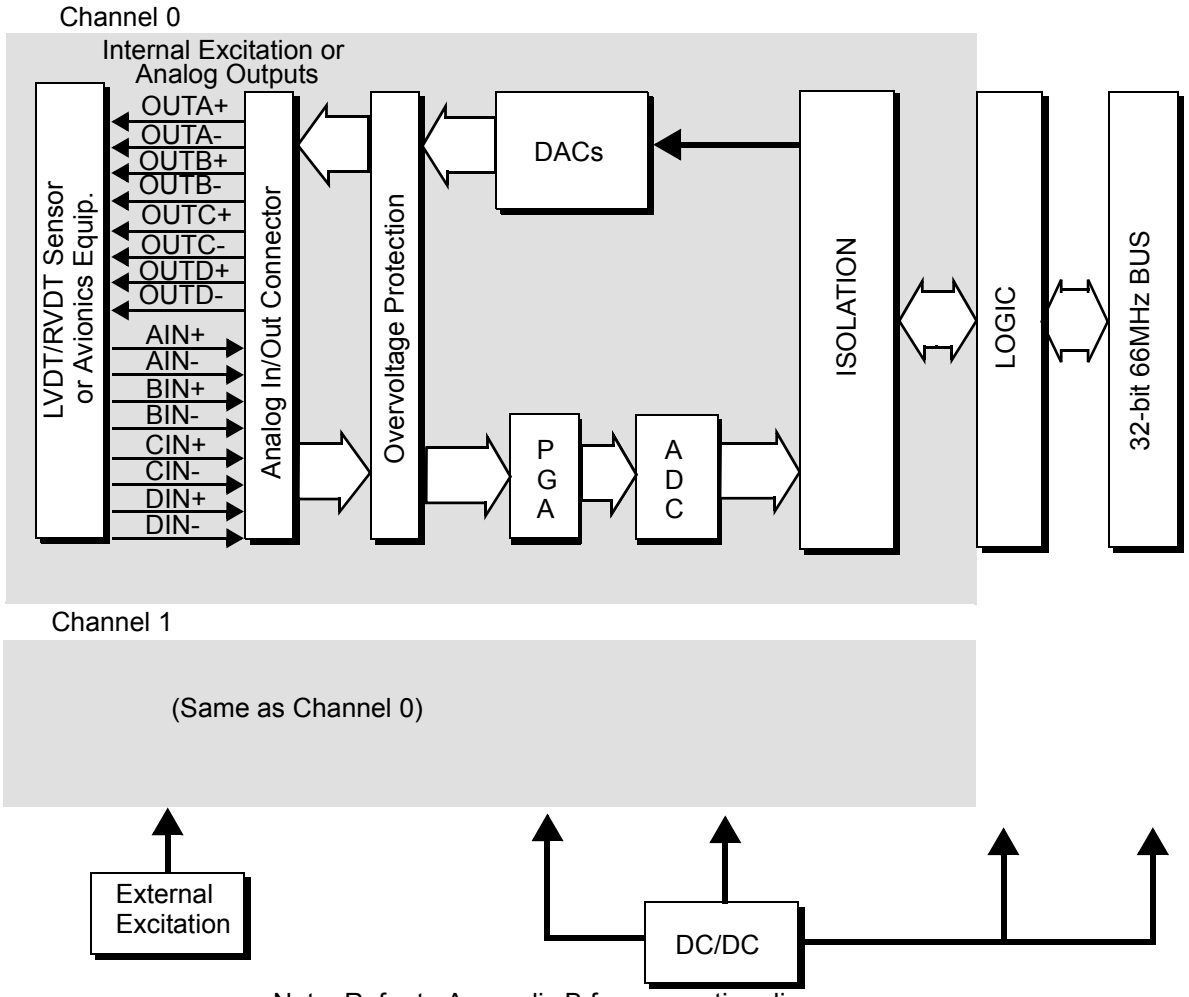
2.3 Device Architecture

A logical block diagram of a AI-256 in LVDT/RVDT mode is shown in **Figure 2-9.**



Note: Refer to Appendix B for connection diagrams

Figure 2-9. Block Diagram of DNx-AI-256 I/O Board

As shown in **Figure 2-9**, board logic is divided into isolated and non-isolated sections. The non-isolated logic complies with the full UEI Common Logic Interface standard. The isolated side handles all functions associated with the sensor input and output circuits.The non-isolated side handles all Cube or chassis-related operations.

Referring to **Fig. 2-9**, the two analog inputs from the synchro or resolver sensor are input to the programmable gain amplifiers (one per input pair) as differential inputs. Selected gain and offset are applied, producing single-ended outputs. These outputs are then converted to differential signals for input to 16-bit SAR analog to digital converters. These converters have serial interface outputs.

The signals from the ADC are passed to a 16-bit quad DAC, combined with $+V_{REF}$ voltage, amplified, and output to a sensor/resolver or avionic hardware. Refer to Appendix B for connection diagrams.

The DACs may be written from multiple sources, such as:

- Direct DAC write registers
- Direct DAC output word register
- Output FIFO. 1024 word FIFO may be used to hold DAC values or commands (in simulation mode)
- Waveform generator — which permits you to output a preloaded waveform on the output channels for simulation purposes
- Combination waveform and FIFO with FIFO in command mode — In this mode, output from FIFO may be directed to phase or gain registers or change may be delayed until the index of waveform is equal to zero.

The logic computes moving averages of all analog inputs (updated with each sample) and also computes other values like (Sa-Sb)/(Sa+Sb) or (Sa-Sb)/Se, where Sa and Sb are computed values of moving averages of analog inputs and Se is the moving average of the excitation voltage value. Timing is controlled by counting pulses in half periods between zero crossings of the reference voltage signal. More information about the computations performed is available in Chapters 3 and 4 and the API Reference Manuals that describe the high-level and low-level functions used with this layer.

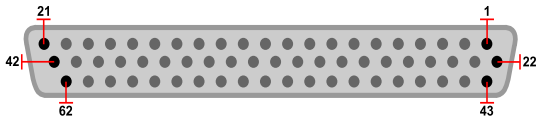
2.4 Setting Operating Parameters

For detailed instructions for configuring the board and setting operating modes and parameters, refer to the applicable functions, which are described in upcoming chapters and also in the PowerDNA API Reference Manual.

2.5 Pinout

The pinout of the DNx-AI-256 62-pin DB connector is shown in **Figure 2-10.**

Pinout Diagram (Synchro/Resolver):



	Pin	Signal	Pin	Signal	Pin	Signal
Chan 0	1	Rsvd	22	Gnd	43	Out A-
	2	Out B+	23	Out B-	44	Out A+
	3	Rsvd	24	n/c	45	Gnd
	4	In A+	25	In A-	46	Rsvd
	5	In B+	26	In B-	47	n/c
	6	Gnd	27	Rsvd	48	Rsvd
	7	Out C+	28	Out C-	49	Rsvd
	8	Out D+	29	Out D-	50	Rsvd
	9	In C+	30	In C-	51	Gnd
	10	In D+	31	In D-	52	Rsvd
	11	Rsvd	32	n/c	53	Out A-
	12	Out B+	33	Out B-	54	Out A+
	13	Rsvd	34	Gnd	55	Gnd
	14	In A+	35	In A-	56	Rsvd
	15	In B+	36	In B-	57	n/c
Chan 1	16	Gnd	37	Rsvd	58	Rsvd
	17	Out C+	38	Out C-	59	n/c
	18	Out D+	39	Out D-	60	Rsvd
	19	Rsvd	40	Gnd	61	In C-
	20	In D+	41	In D-	62	In C+
	21	Rsvd	42	n/c		

Dashed Line represents the isolation barrier between channels

Figure 2-10. Pinout Diagram for the AI-256

Before plugging any I/O connector into the Cube or RACKtangle, be sure to remove power from all field wiring. Failure to do so may cause severe damage to the equipment.

2.6 Synchro-Resolver Wiring Connections

The table shown below (**Table 2-2**) matches the terminal connections of the AI-256 with the corresponding terminals on a synchro or a resolver device or simulator in each of the various operating modes.

For a synchro, the terminals are S1, S2, S3 and C for the three stator windings and common and R1, R2 for the rotor. For a resolver, the terminals are S1/S3 and S2/S4 for stator windings and R1/R2 for the rotor. Exc+ and Exc– refer to excitation. For Connection Diagrams of the various modes, see Appendix B.

Table 2-2. Synchro-Resolver Wiring Connections for Various Modes

Signal Name	Pin No.		Input Mode, Internal Excitation		Input Mode, External Excitation		Simulator Mode, Internal Excitation		Simulator Mode, External Excitation	
	Ch 0	**Ch 1**	*Synchro*	*Resolver*	*Synchro*	*Resolver*	*Synchro*	*Resolver*	*Synchro*	*Resolver*
In A+	4	14	S1	S1	S1	S1	NC	NC	NC	NC
In A-	25	35	C	S3	C	S3	NC	NC	NC	NC
In B+	5	15	S3	S2	S3	S2	NC	NC	NC	NC
In B-	26	36	C	S4	C	S4	NC	NC	NC	NC
In C+	9	62	S2	NC	S2	NC	NC	NC	NC	NC
In C-	30	61	C	NC	C	NC	NC	NC	NC	NC
In D+	10	20	NC	NC	Exc+	Exc+(R1)	NC	NC	Exc+	Exc+
In D-	31	41	NC	NC	Exc-	Exc-(R2)	NC	NC	Exc-	Exc-
OutA+	44	54	NC	NC	NC	NC	S1	S1	S1	S1
OutA-	43	53	NC	NC	NC	NC	C	S3	C	S3
OutB+	2	12	NC	NC	NC	NC	S3	S2	S3	S2
OutB-	23	33	NC	NC	NC	NC	C	S4	C	S4
OutC+	7	17	NC	NC(R2)	NC	NC	S2	Opt+(R2)	S2	NC
OutC-	28	38	NC	NC(R4)	NC	NC	C	Opt-(R4)	C	NC
OutD+	8	18	R1	R1	NC	NC	Exc+	Exc+(R1)	NC	NC
OutD-	29	39	R2	R3	NC	NC	Exc-	Exc-(R3)	NC	NC
NC	24,47	32, 42, 57, 59	--	--	--	--	--	--	--	--
GND	6, 22, 45, 51	16, 34, 40, 55	--	--	--	--	--	--	--	--
Rsvd	1, 3, 27, 46, 48, 49, 50, 52	11, 13, 19, 21, 37, 56, 58, 60	--	--	--	--	--	--	--	--

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2.6.0.1 Line-to-Line & Peak-to-Peak Measurement

The AI-256 performs measurement and stimulation to attached synchros and resolvers by comparing each of the inputs (S1, S2, S3) to a ground reference line at the AI-255's ADC using peak-to-peak voltage (V_{pp}) values.

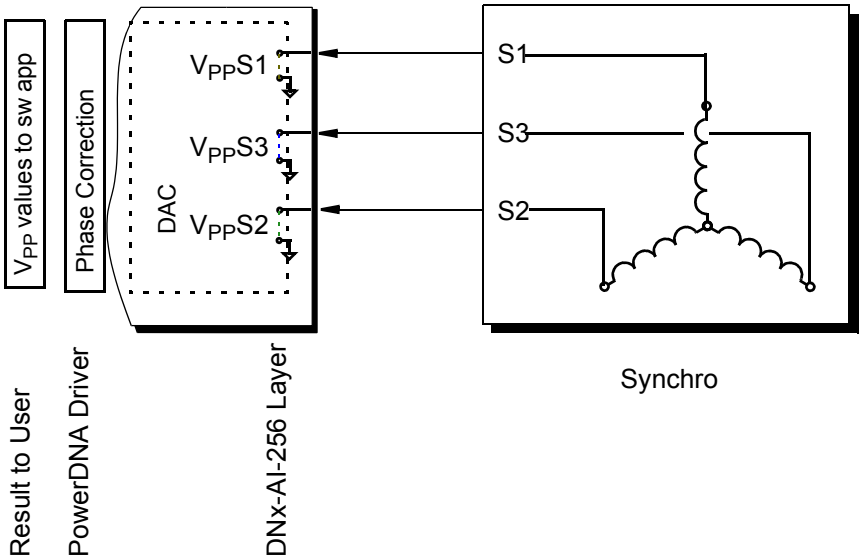

Figure 2-11. Peak-to-peak voltage measurement of Synchro

The synchro, however, is most commonly rated to use the root mean squared (rms) voltage as measured between two lines (not ground referenced). This is the rms line to line voltage (V_{LL}) measured across two of the three stator wires (V_{S1-3}, V_{S3-2}, or V_{S2-1}; as seen on page 8) or the excitation wires (V_{ext+}, V_{ext-}).

The user must convert between the line-to-line RMS voltage amplitude (V_{LL}) from the synchro specification and the peak-to-peak output-to-ground voltage amplitude (V_{PP}) that is the parameter needed by the AI-256 driver.

Convert between V_{LL} and V_{PP} with the relation:

$$V_{PP} = 2\sqrt{2}\frac{V_{LL}}{2\sin(120°)} \cong 1.63299 V_{LL}$$

or using the low-level software macro from *powerdna.h*:

```
#define DQ_AI255_RMS_LN_LN_TO_PP(V) ((V)*1.633)
```

where input parameter V is V_{LL}, and the resulting output is V_{PP}.

Additionally, the low-level API also defines a macro to convert from V_{LL} to V_{RMS}:

```
#define DQ_AI255_RMS_LN_LN_TO_RMS(V) ((V)*0.5774)
```

where input parameter V is the line-to-line voltage V_{LL}, and the result is in volts RMS referenced to ground (V_{RMS}). The constant 0.5774 is 1/(2·sin(120º)).

As an example, a synchro with the rms excitation voltage of 19.8V between V_{ext+} and V_{ext-} will need a ground-referenced peak-to-peak voltage of 56.0V set for the AI-256, since 56.0V ≈ 2·√(2)·19.8V (no phase adjustment necessary). The same synchro's rms stator voltage of 11.8V that is the rms voltage between any two stator connections (responsible for positioning the rotor) should have a maximum peak-to-peak voltage span of 19.26V ≈ 11.8V/1.633·2·√(2).

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Exercise caution when wiring and double-check that correct voltage is set on the AI-256 to avoid overloading and permanently damaging the synchro or resolver.

In Figure 2-11 on page 19, once the data has been sampled, the Cube logic corrects the phase by subtracting 30º, 150º, and 270º from S1, S2, and S3 resulting waveforms to yield an ideal voltage representation. This transformation is transparent, the final result appears as the final V_{PP} value to user application.

2.6.0.2 Z-grounded mode

It is possible to ground the z (S3) lines of some synchros to the vehicle's common ground to save on wiring - this is called a synchro in *z-grounded mode*. For z-grounded synchros, the S3 input/output on the AI-256 is left unconnected. The mode must be set for the AI-256 in software when using z-grounded mode. The modes for the low-level API are listed in the table below; refer to **Chapter 4** for information on low-level software programming.

Mode of Operation	Description
DQ_AI255_MODE_SI_INTZ	Synchro input, int. exc., Z grounded
DQ_AI255_MODE_SI_EXTZ	Synchro input, ext. exc., Z grounded
DQ_AI255_MODE_SS_INTZ	Synchro output, int. exc., Z grounded
DQ_AI255_MODE_SS_EXTZ	Synchro output, ext. exc., Z grounded

Table 2-3. Z-grounded modes of operation from powerdna.h

The connection diagram for wiring a synchro in z-grounded mode is as follows:

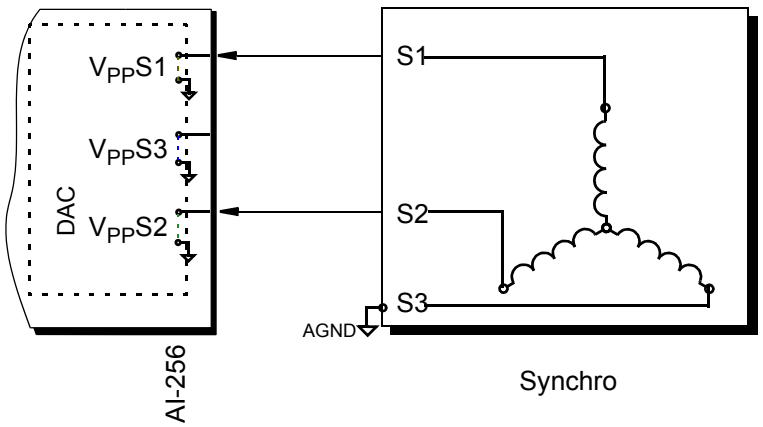

Figure 2-12. Connection in Z-grounded mode of Synchro

2.6.0.3 Trouble-shooting

This section describes some of the symptoms observed when the synchro is not wired correctly to the layer. Incorrect wiring can be as mild as inaccurate rotor position or as severe as permanently damaging the synchro.

In the mildest cases, the synchro or rotor lines may be in incorrect positions in the terminal panel. Reversing the rotor (V_{ext+}, V_{ext-}) or stator (S1, S2, S3) wires can cause the position of the rotor to be at a wrong angle, or rotate clockwise.

In the more severe cases, the rotor may move in a jerky or erratic manner, the synchro may hum and may be warm/hot to the touch, indicating a possible open connection. Warm or hot synchro's may also also indicate a short circuit.

Whereas the layer does have overvoltage protection up to $350V_{RMS}$ and thermal protection, the synchro may be permanently damaged by a bad voltage setting. It is recommended to check the configured voltage with an oscilloscope (best set to measure in true RMS mode) to ensure that the output voltages are correct. Unusual waveforms on an oscilloscope may indicate that thermal limits are being reached (normally due to an overloaded synchro), and waveforms that drop to zero may indicate that the overvoltage protection was breached and the layer has shut down. Overvoltage messages will appear on the serial console and also returns as STS_POST_OVERCURRENT in the POST word of the layer status of the low level framework; refer to **Chapter 4** for information on low-level software programming.

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Chapter 3 LVDT/RVDT Simulator Mode

This document outlines the feature set and use of the DNA-AI-256 Interface board when used in LVDT/RVDT applications only.

3.1 DNx-AI-256 Layer when used with LVDT/RVDTs

The DNx-AI-256 can be used as a 2-channel simulated LVDT/RVDT output interface for UEI's PowerDNA and PowerDNR data acquisition systems. It is suited for a wide variety of linear and rotational motion and/or position measurements in industrial and military applications. Each of the two channels may be configured as an LVDT/RVDT simulator output with internal or external excitation. Each simulated output may be used as a software-controlled input stimulus for an avionics test system or flight simulator.

The wiring connections for the various modes of operation are described in detail in "Operating Modes" on page 26.

Each output channel has four independent 16-bit DACs (total of eight per layer) that permit the channel to be used for outputting two single-ended voltages. Each output channel may be configured to output a simulated output voltage from the secondary of an LVDT/RVDT. When used in the simulator mode, the layer uses a software-defined value as the position input for a simulated LVDT/RVDT device. Each analog output can also generate pre-loaded voltage waveforms with programmable phase shift.

3.2 Specifications

Technical specifications for the DNx-AI-256 board (LVDT/RVDT Mode) are listed in **Table 3-1** and extend the features presented in Chapter 1.

Table 3-1. DNx-AI-256 (LVDT/RVDT Mode) Specifications

Simulation Outputs	
Number of channels	2
Configuration	2-, 3- or 4-wire
Resolution	16-bit
Output Accuracy	0.1%
Output Voltage	19.8Vrms (max)

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3.3 Device Architecture

A block diagram of a DNx-AI-256 board is shown in **Figure 3-1.**

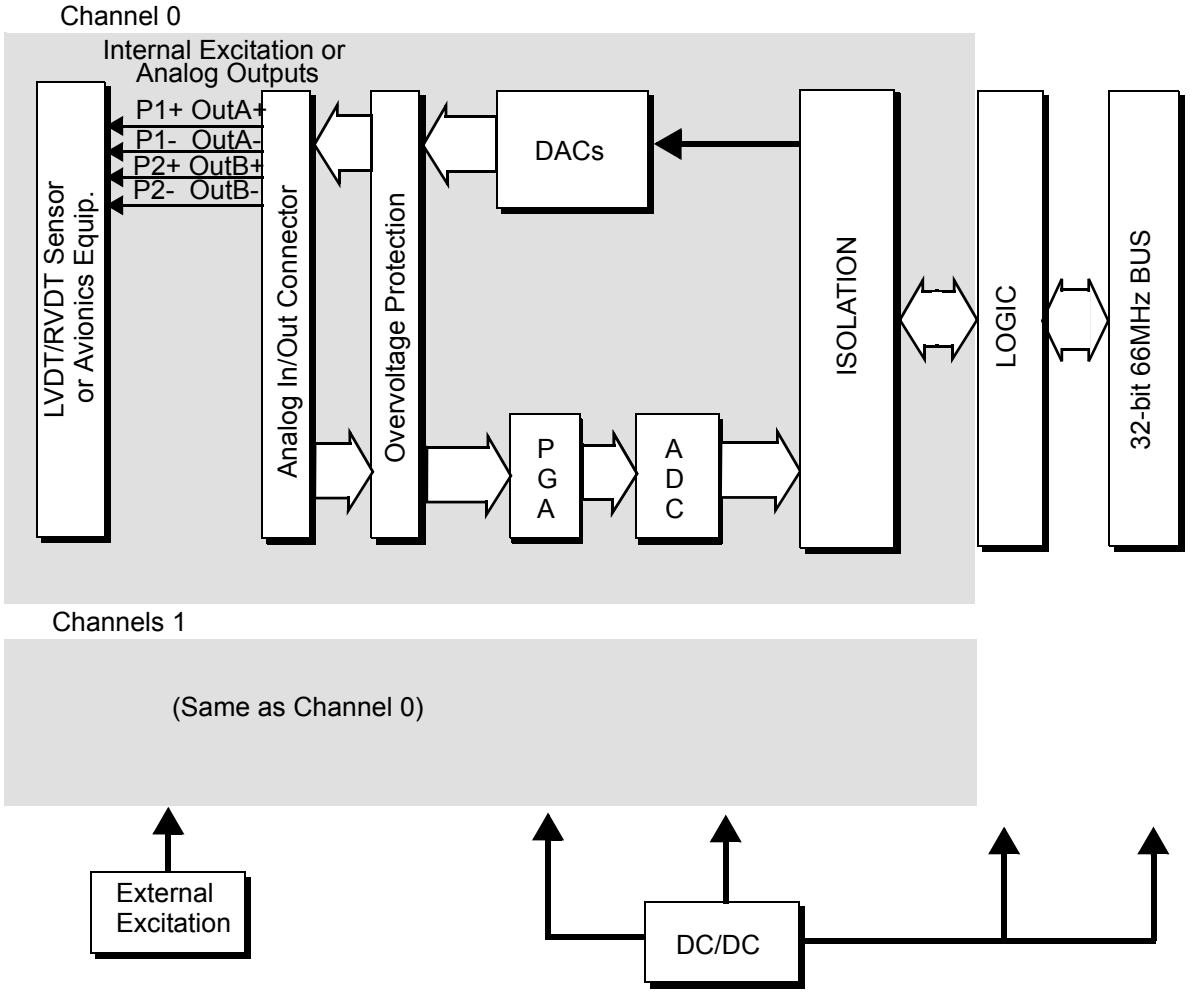

Figure 3-1. Block Diagram of DNx-AI-256 I/O Board

As shown in **Figure 3-1**, board logic is divided into isolated and non-isolated sections. The non-isolated logic complies with the full Common Layer Interface standard. The isolated side handles all functions associated with processing the LVDT/RVDT analog inputs and outputs.

3.3.1 Functional Description

Any channel can be configured as an exclusive LVDT/RVDT simulator output. Examples of the various connections and modes of operation are described later in this chapter. (See **Figure 3-3** to **3-5**)

In Analog Output Mode, when a channel is configured as an LVDT output device, it can simulate the operation of an LVDT/RVDT, outputting DAC-generated analog voltages on P1+, and P2+, as shown in **Figure 3-3** on page 26 and **Figure 3-4** on page 27. It can also be configured to generate a user-defined custom analog waveform output signal on the P1 and P2 terminals normally used for LVDT/RVDT excitation voltage. (Refer “Use of Custom Waveform Output” on page 27.) Timing of the analog waveform output is controlled by detecting zero crossings of the analog input (A_{in}) on the channel.

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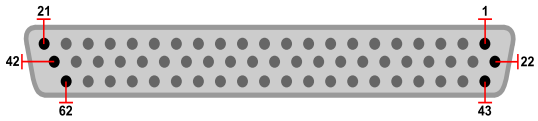
3.4 Pinout

The pinout for the AI-256 in LVDT/RVDT mode is illustrated below:

Pinout Diagram (LVDT/RVDT Mode):



	Pin	Signal	Pin	Signal	Pin	Signal
Chan 0	1	Rsvd	22	Gnd	43	Out A- (P1-)
	2	Out B+ (P2+)	23	Out B- (P2-)	44	Out A+ (P1+)
	3	Rsvd	24	n/c	45	Gnd
	4	In A+ (S1+)	25	In A- (S1-)	46	Rsvd
	5	In B+ (S2+)	26	In B- (S2-)	47	n/c
	6	Gnd	27	Rsvd	48	Rsvd
	7	Out C+	28	Out C-	49	Rsvd
	8	Out D+	29	Out D-	50	Rsvd
	9	In C+	30	In C-	51	Gnd
	10	In D+	31	In D-	52	Rsvd
Chan 1	11	Rsvd	32	n/c	53	Out A- (P1-)
	12	Out B+ (P2+)	33	Out B- (P2-)	54	Out A+ (P1+)
	13	Rsvd	34	Gnd	55	Gnd
	14	In A+ (S1+)	35	In A- (S1-)	56	Rsvd
	15	In B+ (S2+)	36	In B- (S2-)	57	n/c
	16	Gnd	37	Rsvd	58	Rsvd
	17	Out C+	38	Out C-	59	n/c
	18	Out D+	39	Out D-	60	Rsvd
	19	Rsvd	40	Gnd	61	In C-
	20	In D+	41	In D-	62	In C+
	21	Rsvd	42	n/c		

Dashed Line represents the isolation barrier between channels

Note:
InA+, InA-, InB+, InB-, InC+, InC-, are not used.

Figure 3-2. DNx-AI-256 LVDT/RVDT Pinout Diagram

NOTE:

1. P1+ represents the output of DACs. They may be used as single-ended voltage outputs. When the AI-256 is configured for internal excitation, they are normally used to provide the excitation voltage for an LVDT/RVDT device. When the AI-256 is configured in simulation mode, P1+ is used to provide one of the two simulated measurement outputs (S1 secondary).
2. P2+ represents the output of DACs. They may be used as single-ended voltage outputs. When the AI-256 is configured for internal excitation, they are normally not used or connected. When the AI-256 is configured in simulation mode, P2+ is used to provide the second of the two simulated measurement outputs (S2 secondary).

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The following table is provided as a convenient reference for connecting sensors to the various I/O pins.

Table 1-1. DNx-AI-256 Pin Connections by Channel Number

Signal Name	Input/Output	Ch 0	Ch 1
P1+	OutA+	44	54
P1-	OutA-	43	53
P2+	OutB+	2	12
P2-	OutB-	23	33
Exc+	InD+	10	20
Exc-	InD-	31	41
Exc+	OutD+	8	18
Exc-	OutD-	29	39
Rsvd	Rsvd	1, 3, 27, 46,48, 49, 50	11, 13, 19, 21, 37, 56, 58, 60
NC	NC	24, 27, 47,	32, 42, 57, 59
Gnd	Gnd	22, 45, 51	16, 34,40, 55

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3.5 Operating Modes

The DNx-AI-256 (LVDT/RVDT Mode) can be used in any of four operating sub-modes, as follows:

- (Mode5) Simulation of the outputs of a 6-wire LVDT/RVDT with external excitation
- (Mode6) Simulation of the outputs of a 4-wire LVDT/RVDT with external excitation
- Mode 7 6-wire simulation with internal excitation
- Mode 8 4-wire simulation with internal excitation

3.5.1 Simulator Output Mode with External Excitation

If configured as a LVDT/RVDT simulator output, a channel can output signals with 16-bit resolution that simulate the two secondary outputs of an LVDT/RVDT and that correlate to the calculated position of the magnetic core of a software simulated LVDT/RVDT device. Excitation voltage is supplied from an external source both to the avionics equipment and to the InD+ and InD- pins on the AI-256, where it used as a reference. Simulation of a 4-wire device in mode 6 is shown in **Figure 3-3.**

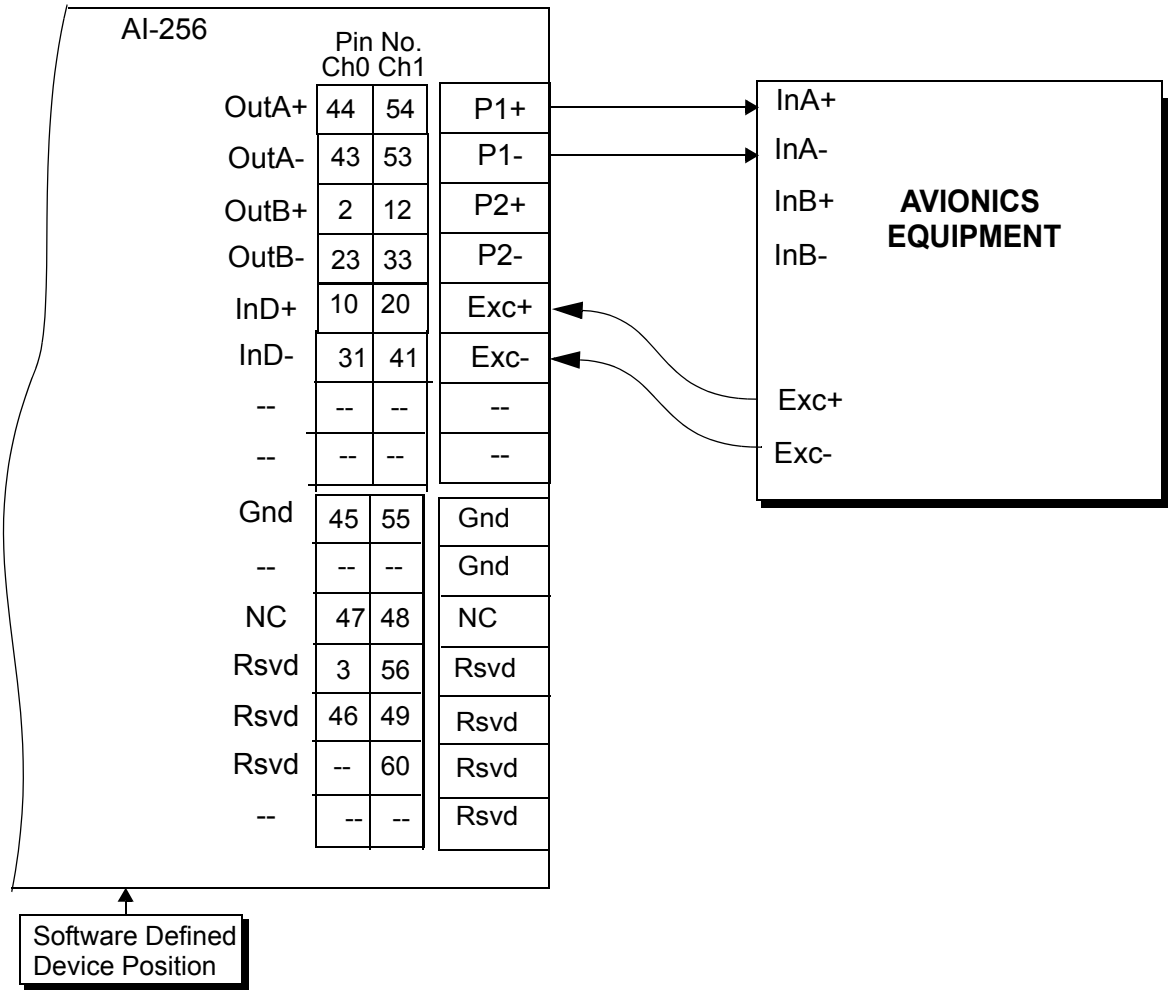

Figure 3-3. 4-wire LVDT Device with AI-256 in Simulator Mode

Simulation of a 5/6-wire device (mode 5) is shown in **Figure 3-4.**

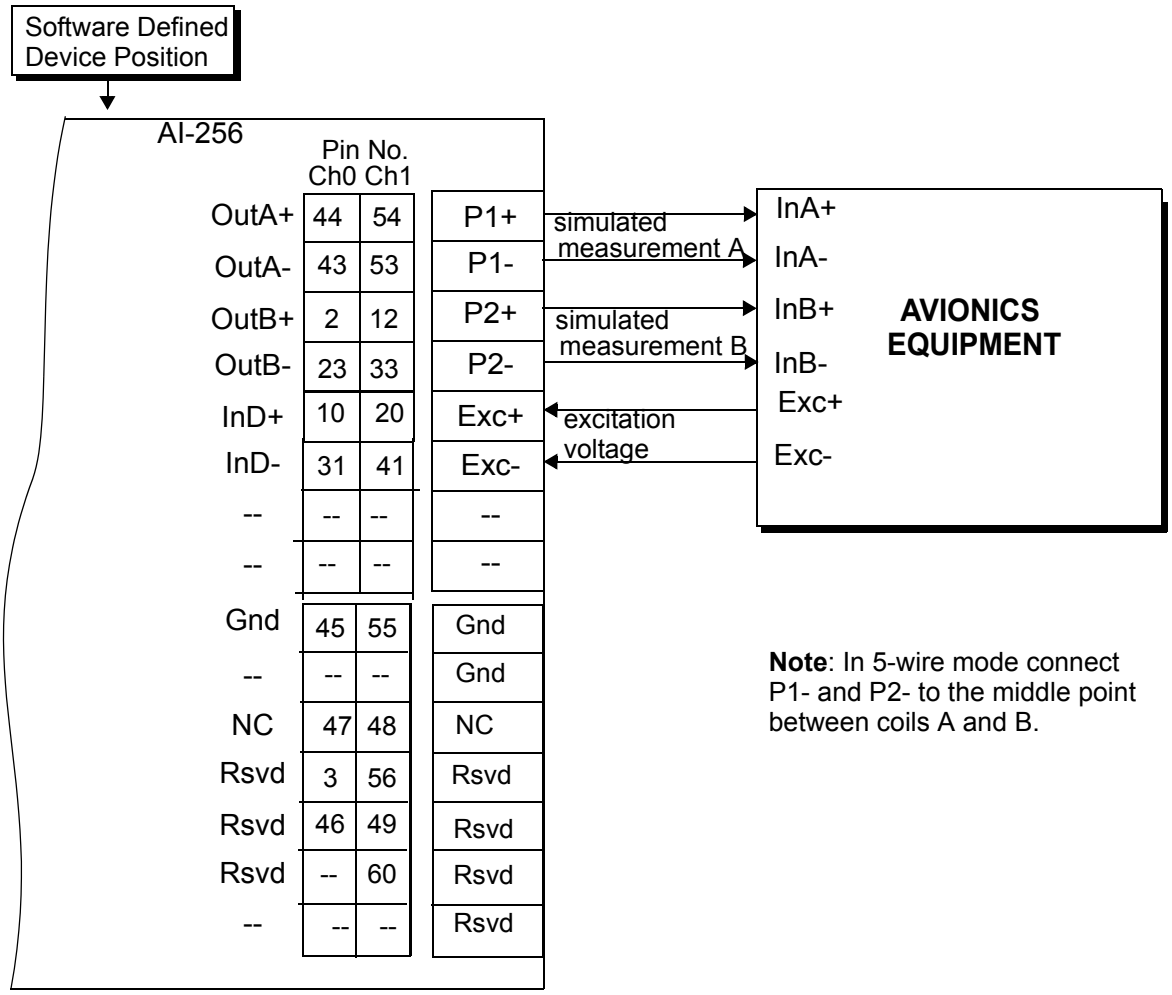

Figure 3-4. 5/6-wire LVDT Device with AI-256 in Simulator Output Mode, External Excitation

3.5.2 Use of Custom Waveform Output

In some situations, such as testing the effect of a particular harmonic in an excitation signal, it may be useful to use a custom waveform (with programmable phase shift) instead of a standard sine wave for the excitation signal. In such cases, you can use the **DqAdvSetWForm( )** function instead of the **DqAdv254SetExcitation( )** function. The AI-256 will then output the custom waveform on excitation channels P1 and/or P2. For detailed information, refer to Chapters 3 and 4 of this manual, to the UEI Framework Reference Manual, or to the UEI PowerDNA API Reference Manual.

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3.5.3 Simulator Output to LVDT/RVDT Input Mode

As shown in the diagram, excitation voltage is provided by Channel 0 (P1+ to P1-) DAC. The Ch0 (P2+ to P2-) DAC output is zero. Channel 1 outputs two simulated measurement signals (P1+ to P1-) and (P2+ to P2-) from its DACs to the secondary inputs on Channel 0.

The figure below is a 4-wire AI-256 on in simulation output mode6 with external excitation connected to a 4-wire AI-254 in input mode1 with internal excitation as described above.

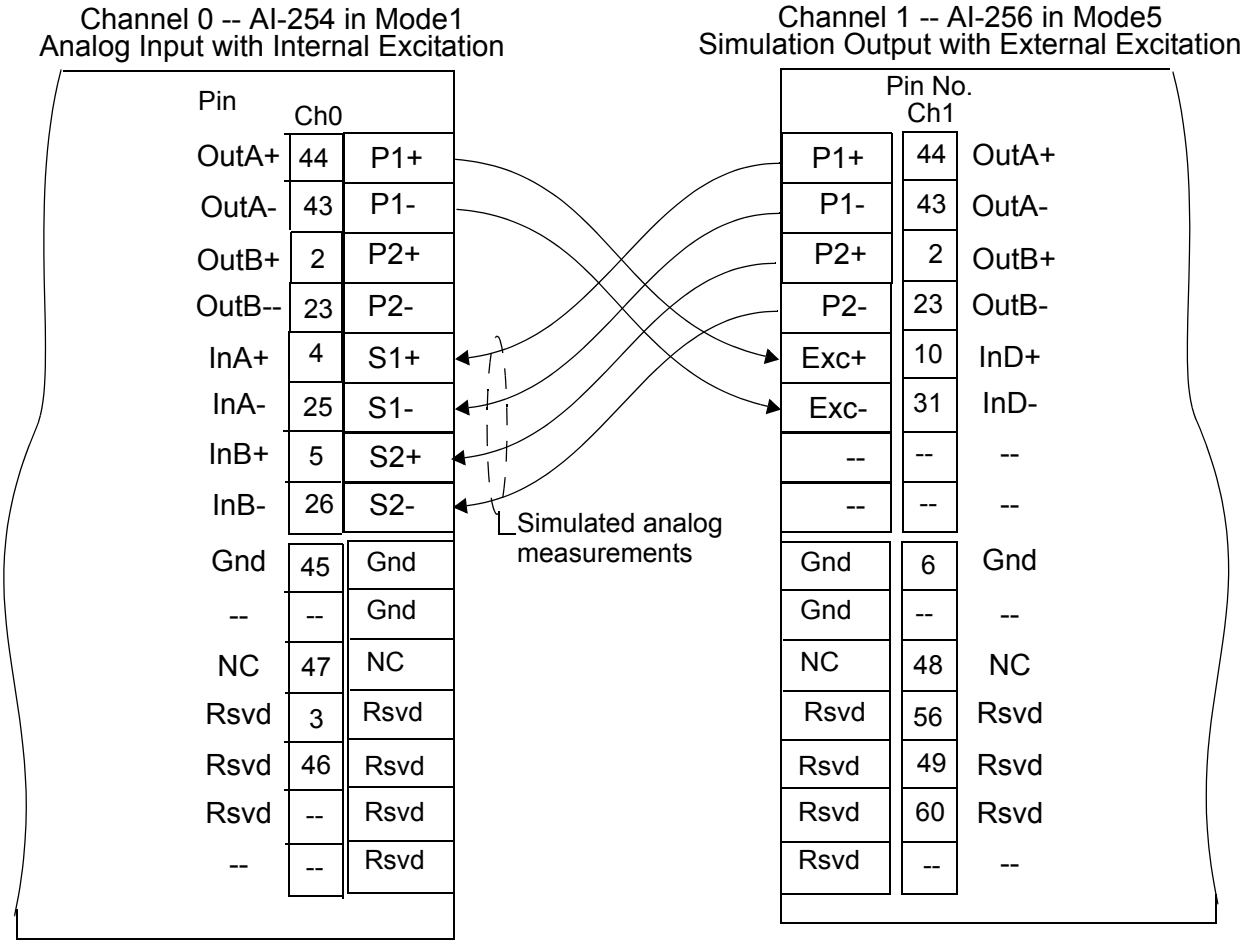

Figure 3-5. AI-256 in Simulation Output mode connected to AI-254 in Analog Input mode

3.6 Setting Operating Parameters

For detailed instructions for configuring the board and setting operating modes and parameters for AI-256 (LVDT/RVDT Mode), refer to the Framework function **CreateSimulatedLVDTChannel** or the low level API Functions **DqAdv254SetMode** or equivalent **DqAdv256SetModeLvdt**.

Framework functions are described in the Framework API Reference Manual; low level functions are described in the PowerDNA API Reference Manual; an overview is covered in the upcoming two chapters.

Chapter 4 Programming with the High Level API

This section describes how to control the DNx-AI-256 using the UeiDaq Framework High Level API.

UeiDaq Framework is object oriented and its objects can be manipulated in the same manner from different development environments such as Visual C++, Visual Basic or LabVIEW.

The following section focuses on the C++ API, but the concept is the same no matter what programming language you use.

Please refer to the “UeiDaq Framework User Manual” for more information on use of other programming languages.

4.1 Creating a Session

The Session object controls all operations on your PowerDNx device. Therefore, the first task is to create a session object:

```
// create a session object for input, and a session object for output

CUeiSession aiSession;
CUeiSession aoSession;
```

4.2 Configuring the Resource String

UeiDaq Framework uses resource strings to select which device, subsystem and channels to use within a session. The resource string syntax is similar to a web URL:

```
<device class>://<IP address>/<Device Id>/<Subsystem><Channel list>
```

For PowerDNA and RACKtangle, the device class is **pdna**.

For example, the following resource string selects analog output lines 0,1 on device 1 at IP address 192.168.100.2: “pdna://192.168.100.2/Dev1/Ao0:1”

4.3 Configuring for Input

The AI-256 can be configured for synchro/resolver input.

When working with synchro/resolvers, use the method **CreateSynchroResolverChannel()** to program the input channels and parameters associated with each channel. (Refer to AI-255 API for details.)

The following call configures the analog input channels of an AI-256 set as device 1:

```
// Configure session synchro/resolver input

aiSession.CreateSynchroResolverChannel(
                                    "pdna://192.168.100.2/Dev1/Ai0,1",
                                     UeiSynchroMode,
                                     3.0,
                                     5000.0,
                                     false);
```

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It configures the following parameters:

- **Sensor Mode**: the type of sensor (synchro or resolver) connected to the input channel.
- **Excitation Voltage**: the amplitude of the excitation sine wave in volts RMS.
- **Excitation Frequency**: the frequency of the excitation sine wave.
- **External Excitation**: specifies whether you wish to provide external excitation or use the excitation provided by the AI-256.

If you want to use different parameters for each channel, you can call **CreateSynchroResolverChannel()** multiple times with a different set of channels (0 or 1) in the resource string.

4.4 Simulated Synchro/ Resolver Output

The AI-256 can be configured for synchro/resolver output. When using the AI-256 in Synchro/Resolver Mode, you can also use the AI-256 to simulate a Synchro or a Resolver output.

The following call configures an analog output channel of an AI-256 set as device 1:

```
// Configure session for synchro/resolver output

aoSession.CreateSimulatedSynchroResolverChannel(
                                    "pdna://192.168.100.2/Dev1/AO0",
                                     UeiResolverMode,
                                     3.0,
                                     5000.0,
                                     false);
```

It configures the following parameters:

- **Sensor Mode**: the type of sensor (synchro or resolver) to be simulated.
- **Excitation Voltage**: the amplitude of the excitation sine wave in volts RMS.
- **Excitation Frequency**: the frequency of the excitation sine wave.
- **External Excitation**: specifies whether you wish to provide external excitation or use the excitation provided by the AI-256.

4.5 Simulated LVDT Output

You can also use the AI-256 to simulate an LVDT or RVDT output.

The following call configures an Analog output channel on a AI-256 set as device 1:

```
// Configure session for synchro/resolver output

aoSession.CreateSimulatedLVTDChannel(
                                    "pdna://192.168.100.2/Dev1/AO0",
                                     153.65
                                     UeiLVDTFiveWires,
                                     3.0,
                                     5000.0,
                                     false);
```

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It configures the following parameters:

- **Sensor Sensitivity**: the sensor sensitivity specified in mV/V/<position unit>. The position unit specifies the unit of the data written to the channel.
- **Wiring Scheme**: the wiring scheme used to connect the simulated LVDT/RVDT to the reading device.
- **Excitation Voltage**: the amplitude in volt RMS of the excitation sine wave.
- **Excitation Frequency**: the frequency of the excitation sine wave.

4.6 Configuring the Timing

You can configure the AI-256 to run in simple mode (point by point), buffered mode (ACB mode), or DMAP mode.

NOTE: ACB (buffered) mode is not currently supported for the AI-256, but will be available in the near future. If you have a specific need for this feature, please contact UEI for current availability status

In simple mode, the delay between samples is determined by software on the host computer. In DMAP mode, the delay between samples is determined by the AI-256 on-board clock and data is transferred one scan at a time between PowerDNA and the host PC. In buffered mode, the delay between samples is determined by the AI-256 on-board clock and data is transferred in blocks between PowerDNA and the host PC.

The following sample shows how to configure the simple mode. Please refer to the “UeiDaq Framework User’s Manual” to learn how to use other timing modes.

```
// configure timing of input for point-by-point (simple mode)
aiSession.ConfigureTimingForSimpleIO();
// configure timing of output for point-by-point (simple mode)
aoSession.ConfigureTimingForSimpleIO();
```

4.7 Read Data

Reading data is done using *reader* object(s). The following sample code shows how to create a scaled reader object and read samples.

```
// create a reader and link it to the analog-input session’s stream
CUeiAnalogScaledReader aiReader(aiSession.GetDataStream());
// the buffer must be big enough to contain one value per channel
double data[2];
// read one scan
aiReader.ReadSingleScan(data);
```

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4.8 Write Data

Writing data is done using a *writer* object.

The following sample shows how to create a scaled writer and write samples. The AI-256 simulates angle positions entered in radians.

```
// create a writer and link it to the session's analog-output stream
CUeiAnalogScaledWriter aiWriter(aoSession.GetDataStream());
// to write a value, the buffer must contain one value per channel
double data[2] = { 1.0, 2.0 };
// write one scan, the buffer must contain one value per channel
aoWriter.WriteSingleScan(data);
```

4.9 Cleaning-up the Session

The session object will clean itself up when it goes out of scope or when it is destroyed. To reuse the object with a different set of channels or parameters, you can manually clean up the session as follows:

```
// clean up the sessions
aiSession.CleanUp();
aoSession.CleanUp();
```

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Chapter 5 Programming with the Low-level API

This chapter illustrates how to program the PowerDNA cube using the low-level API. The low-level API offers direct access to PowerDNA DAQBios protocol and also allows you to access device registers directly.

However, we recommend that, when possible, you use the UeiDaq Framework High-Level API (see Chapter 4), because it is easier to use. You should need to use the low-level API only if you are using an operating system other than Windows.

NOTE: This chapter contains descriptive information about the various operating modes and wiring connections of the AI-256, and descriptions of the low-level functions that may be used in programming this module. When you use the AI-256 with synchros and resolvers, use the functions listed in the API chapter for the AI-255; when you use it with LVDTs or RVDTs, use the functions listed for the AI-254. Note, however, that the AI-256 only has 2 channels rather than four channels as with the AI-254 and AI-255.

For additional information about low-level programming of the AI-256, please refer to the PowerDNA API Reference Manual document under:

Start » Programs » UEI » PowerDNA » Documentation

5.1 DNx-AI-256 Modes of Operation

The six modes of operation supported by an DNx-AI-256 channel are:

- Synchro Input
- Resolver Input
- Synchro Output/Simulator
- Resolver Output/Simulator
- LVDT Simulator Output
- RVDT Simulator Output

Synchro and Resolver modes of operation are described in **Section 5.2**, and the LVDT and RVDT output modes of operation are described in **Section 5.3**.

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5.2 Using the AI–256 with Synchro/ Resolver Devices

This section describes the use of the AI-256 in Synchro/Resolver applications.

For applications that use LVDTs and RVDTs, refer to “Using the AI–256 with LVDT/RVDT Devices” on page 38.

There are eight Synchro/Resolver modes of operation. Functions performed by these modes of operation supported by this layer may be described as follows:

- **Synchro Input with internal excitation**: The AI-256 reads the voltages on the stator coils as analog inputs and also supplies the excitation voltage to the rotor coil.
- **Synchro Input with external excitation:** The AI-256 reads the voltages on the stator coils as analog inputs. An external source supplies the excitation voltage to the rotor coil, which is readback by the AI-256 as an analog input.
- **Resolver Input with internal excitation**: The AI-256 reads the voltages on the stator coils as analog inputs and also supplies the excitation voltage to the rotor coil(s).
- **Resolver Input with external excitation:** The AI-256 reads the voltages on the stator coils as analog inputs. An external source supplies the excitation voltage to the rotor coil(s), which is readback by the AI-256 as an analog input.
- **Synchro Simulation with internal excitation:** The AI-256 outputs voltages that simulate the analog signals from stator coils of a synchro. It also outputs an analog excitation voltage generated in the AI-256.
- **Synchro Simulation with external excitation:** The AI-256 outputs voltages that simulate the analog signals from stator coils of a synchro. Excitation voltage is supplied by an external source and read back by the AI-256 as an analog input.
- **Resolver Simulation with internal excitation:** The AI-256 outputs voltages that simulate the analog signals from stator coils of a resolver. It also outputs an analog excitation voltage generated in the AI-256.
- **Resolver Simulation with external excitation:** The AI-256 outputs voltages that simulate the analog signals from stator coils of a resolver. Excitation voltage is supplied by an external source and read back by the AI-256 as an analog input.

All the modes available are defined in powerdna.h.
The above eight modes of operation are set by the following definitions:

```
#define DQ_AI255_MODE_SI_INT0  // Synchro input, internal excitation
#define DQ_AI255_MODE_RI_INT1  // Resolver input, int.exc.
#define DQ_AI255_MODE_SI_EXT2  // Synchro input, ext. exc. - readback exc. on D
#define DQ_AI255_MODE_RI_EXT3  // Resolver input, ext. exc. - readback exc. on D
#define DQ_AI255_MODE_SS_INT4  // Synchro drive/simulation, int. exc. - fully sourced
#define DQ_AI255_MODE_RS_INT5  // Resolver drive/simulation, int.exc. - fully sourced
#define DQ_AI255_MODE_SS_EXT6  // Synchro drive/simulation, ext. exc. - readback on D
#define DQ_AI255_MODE_RS_EXT7  // Resolver drive/simulation, ext. exc. - readback on D
```

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5.2.1 Wiring

A synchro has three stator coils S1, S2, S3 connected in a star fashion to the Common. The rotor primary coil (exciter) has wires R1 and R2.

Resolver stator coils are S1-S3 and S2-S4. Rotor coil is R1-R3 (and R2-R4 when two rotor windings are used).

Table 4-1 describes the wiring connections for various modes of operation.

Table 4-1. Wiring Connections for Various Synchro/Resolver Operating Modes

Mode	Synchro (three 120º coils)		Resolver (two 90º coils)	
	AOut	AIn	AOut	AIn
Input, internal excitation, 19.8V_{rms} 400Hz-10kHz.	R1 and R2 connected to D+ and D- (optionally use A, B or C in parallel).	S1 to A+, S3 to B+, S2 to C+.	R1 and R3 connected to D+ and D-, optionally R2 and R4 to C+ and C- (two windings per rotor).	S1 to A+, S3 to A-, S2 to B+, S4 to B-.
Input, external excitation 28V_{rms} (from A/C bus).	N/C	S1 to A+, S3 to B+, S2 to C+, Excitation readback to D+/D-.	N/C	S1 to A+, S3 to A-, S2 to B+, S4 to B-, Excitation readback to D+/D-.
Output, internal excitation, 19.8V_{rms}	S1 to A+, S2 to B+, S3 to C+, R1 to D+, R2 to D- and Common to AGND.	N/C	S1 to A+, S3 to A-, S2 to B+, S4 to B- R1 to D+, R3 to D- and Common to AGND. Optionally, R2 to C+ and R4 to C-.	N/C
Output, external excitation 28V_{rms} (from A/C bus), internal drive (resolver only).	S1 to A+, S2 to B+, S3 to C+ and Common to AGND.	Excitation readback to D+/ D.-	S1 to A+, S3 to A-, S2 to B+ and S4 to B-.	Excitation readback to D+/ D-.

Mode: Input, Internal Excitation

```
DQ_AI255_MODE_SI_INT:
DQ_AI255_MODE_RI_INT:

     exc_rate = 400.0; <- excitation frequency is the same for both calls
     exc_level = 26.0; <- level for the rotor coil (gnd-ref, pk-to-pk, not rms)
                       (you may use the provided macro to convert rms & pk-pk)
     adc_rate = 0; -> returns actual sampling rate
     ret = DqAdv255SetExcitation(hd0, DEVN, CHANNEL,
                                 DQ_AI255_ENABLE_EXC_D, // D channel only
                                 exc_rate, exc_level, &adc_rate);

     exc_level = 26.0; <- level for the rotor coil (from the datasheet)
     ret = DqAdv255SetMode(hd0, DEVN, CHANNEL, mode, flags,
                           (float)exc_rate, (float)exc_level);
```

Mode: Input, External Excitation

```
DQ_AI255_MODE_SI_EXT:
DQ_AI255_MODE_RI_EXT:

// Measure frequency and level on input D
ret = DqAdv255MeasureWF(hd0, DEVN, CHANNEL_COARSE,
                        &exc_rate, &exc_level, &exc_offs);

// use excitation frequency measured on the rotor winding
// use excitation voltage measured on the rotor winding
// this information is required to estimate A/D settings
ret = DqAdv255SetMode(hd0, DEVN, CHANNEL, mode, flags, exc_rate, exc_level);
```

Mode: Output, Internal Excitation

```
DQ_AI255_MODE_SS_INT:
DQ_AI255_MODE_RS_INT:

     exc_rate = 400.0; <- excitation frequency is the same for both calls
     exc_level = 26.0; <- level for the rotor coil (pk-to-pk, not rms)
     adc_rate = 0; -> returns actual sampling rate
     ret = DqAdv255SetExcitation(hd0, DEVN, CHANNEL_SIM,
                                 DQ_AI255_ENABLE_EXC_D, // D channel only
                                 exc_rate, exc_level, &adc_rate);

    exc_level = 11.8; <- level for the stator coils (from the datasheet, pk-pk)
    ret = DqAdv255SetMode(hd0, DEVN, CHANNEL_SIM, mode, flags,
                          (float)exc_rate, (float)exc_level);
```

Mode: Output, External Excitation

```
DQ_AI255_MODE_SS_EXT:
DQ_AI255_MODE_RS_EXT:

// Measure frequency and level on input D
ret = DqAdv255MeasureWF(hd0, DEVN, CHANNEL_COARSE,
                        &exc_rate, &exc_level, &exc_offs);


exc_level = 11.8; <- level for the stator coils (from the datasheet, pk-pk)
ret = DqAdv255SetMode(hd0, DEVN, CHANNEL, mode, flags, exc_rate, exc_level);
```

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5.2.2 Low-Level Functions

The low-level synchro/resolver functions for an AI-256 layer are described in the PowerDNA API Reference Manual Release 4.5, Section 4.9 to 4.11.

The following functions are inherited by the AI-256 from the AI-255 for use with synchro/resolver applications:

Function	Description
DqAdv255SetMode	Sets up one of the S/R operating modes supported by the AI-256.
DqAdv255SetExt	Set up extra (additional) parameters.
DqAdv255SetExcitation	Sets excitation frequency and amplitude in internal exitation mode.
DqAdv255GetWFMeasurements	Returns the measured parameters of waveform on selected input(s).
DqAdv255MeasureWF	Simple form of DqAdv255GetWFMeasurements.
DqAdv255Enable	Refer to DqAdv256Enable.
DqAdv255GetExcitation	Gets layer excitation voltage parameters of excitation waveform.
DqAdv255Read	Read the calculated angle or special data for selected channels.
DqAdv255Write	Write a simulated position of a synchro or resolver or special data.
DqAdv255ConvertSim	Converts angle to raw data representation for gain and phase control.
DqAdv255WriteBin	Writes an angle or special data for selected channels.
DqAdv255ReadDIn	Reads digital inputs.
DqAdv255WriteDOut	Writes digital outputs and reads back digital inputs.

The following AI-256 superset of functions extend the abilities of the AI-255:

Function	Description
DqAdv256SetModeSynchroResolver	Identical to DqAdv255SetMode()
DqAdv256Enable	Enable/disable operations for channels specified in channel list.
DqAdv256WriteSynchroResolver	Identical to DqAdv255Write()
DqAdv256ReadPADC	Returns the power monitor ADC readings from an AI-256 layer.
DqAdv256SetAll	Sets up most of the AI-256 configuration parameters.
DqAdv256GetWFMeasurements	Returns the measured parameters of waveform on the input line(s).

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5.3 Using the AI–256 with LVDT/RVDT Devices

The DNx-AI-256 layer can be configured as a 2-channel all-digital LVDT/RVDT simulator. (**Note**: When used in this mode, the AI-256 uses low level functions for the AI-254.) It has two A/Ds and two D/As per channel, each capable of sampling at a rate up to 330kHz. For simulation, all processing occurs in the digital domain and the D/As convert a digital representation of the simulated signal into an analog waveform at the last stage of the processing.

There are four modes of operation supported by this layer based on simulation mode for LVDT/RVDTs:

- **Simulation mode** (when the layer is connected directly into the avionics and simulates (or mimics) the LVDT sensor itself). This mode is used when an external device expects to receive output from an LVDT sensor in response to an applied excitation voltage. The AI-256 calculates parameters of the externally applied excitation and generates sine-waves on its outputs in accordance with the requested LVDT position.

Simulation mode has two variations:

- **5/6 wire connection:** In case of 5 wire circuitry, connect a common point between coils to both P1- and P2- lines.
- **4 wire connection:** In this case, you have to make sure that the external excitation signal is properly attenuated and applied to the InD input of the AI-256.

The above two variations may use **internal** or **external** excitation.

The four modes of operation are defined in software as:

```
DQ_AI254_MODE_SIM_5          // 254 Mode5: ext. exc. simulation, 5-wire LVDT
DQ_AI254_MODE_SIM_4          // 254 Mode6: ext. exc. simulation, 4-wire LVDT
DQ_AI256_MODE_SIM_5_INT      // 254 Mode7: int. exc. simulation, 5-wire LVDT
DQ_AI256_MODE_SIM_4_INT      // 254 Mode8: int. exc. simulation, 4-wire LVDT
```

The following table summarizes the required connections between an AI-256 layer (in LVDT/RVDT Mode) and an LVDT:

Table 4-2. Wiring between AI-256 (LVDT/RVDT Simulation Mode) and an LVDT input device

Mode	4-wires		5/6-wires	
	AOut	**AIn**	**AOut**	**AIn**
Simulator, external excitation	P1+ and P1- connected to InA+ and InA- of the device	InD+ and InD- connected to Exc+ and Exc- output of the device	P1+ and P1- connected to InA+ and InA- of device; P2+ and P2- connected to InB+ and InB- of device;	InD+ and InD- connected to Exc+ and Exc- output of the device
Simulator, internal excitation	P1+ / P1- to InA+ / InA- of the device; P2+ / P2- to Exc+ / Exc- input of the device		P1+ / P1- to InA+ / InA- of device; P2+ / P2- to InB+ / InB- of device; OutD+ / OutD- to Exc+ / Exc- of dev.	

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5.3.1 LVDT/RVDT Functions

The LVDT/RVDT low-level functions for an AI-256 layer are listed in this section.

The following AI-256 functions perform functions useful to LVDT applications:

Function	Description
DqAdv256SetModeLvdt	Sets one of four LVDT simulation operating modes for 5 or 6 wire, internal or external excitation. Refer to PowerDNA API Ref. Manual.
DqAdv256Enable	Enable/disable operations for channels specified in channel list.
DqAdv256ConvertSimLvdt	Converts a ±1.0 position into raw data representation for gain/phase.
DqAdv256GetWFMeasurements	Returns the measured parameters of waveform on the input line(s).
DqAdv256ReadPADC	Returns the power monitor ADC readings from an AI-256 layer.
DqAdv256SetAll	Sets up AI-256 configuration parameters to non-default variables.
DqAdv256WriteLvdt	Writes simulated position to simulate 4 and 5/6 wire LVDTs.

The following AI-254 functions have AI-256 equivalents (but not vice versa):

Function	Description
DqAdv254SetMode	Identical to DqAdv256SetModeLvdt()
DqAdv254GetWFMeasurements	Identical to DqAdv256GetWfMeasurements()
DqAdv254Enable	Identical to DqAdv256Enable()
DqAdv254Write	Identical to DqAdv256WriteLvdt()
DqAdv254ConvertSim	Identical to DqAdv256ConvertSimLvdt()

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Appendix A

A. Accessories

The following cables and STP boards are available for the AI-256 layer.

DNA-CBL-62

This is a 62-conductor round shielded cable with 62-pin male D-sub connectors on both ends. It is made with round, heavy-shielded cable; 2.5 ft (75 cm) long, weight of 9.49 ounces or 269 grams; up to 10ft (305cm) and 20ft (610cm).

DNA-STP-62

The STP-62 is a Screw Terminal Panel with three 20-position terminal blocks (JT1, JT2, and JT3) plus one 3-position terminal block (J2). The dimensions of the STP-62 board are 4w x 3.8d x1.2h inch or 10.2 x 9.7 x 3 cm (with standoffs). The weight of the STP-62 board is 3.89 ounces or 110 grams.

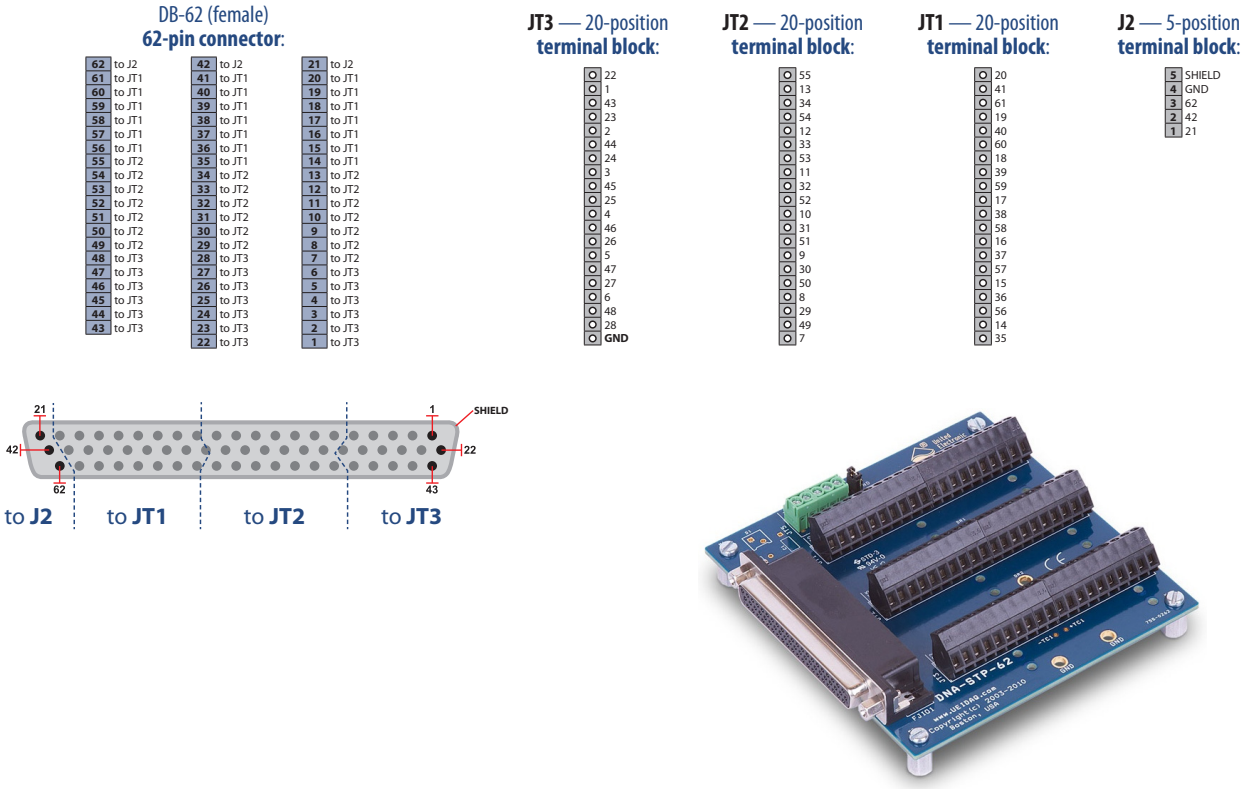


Figure A-1. Pinout and photo of DNA-STP-62 screw terminal panel

Appendix B

Connection Diagrams for S/R Operating and Excitation Modes

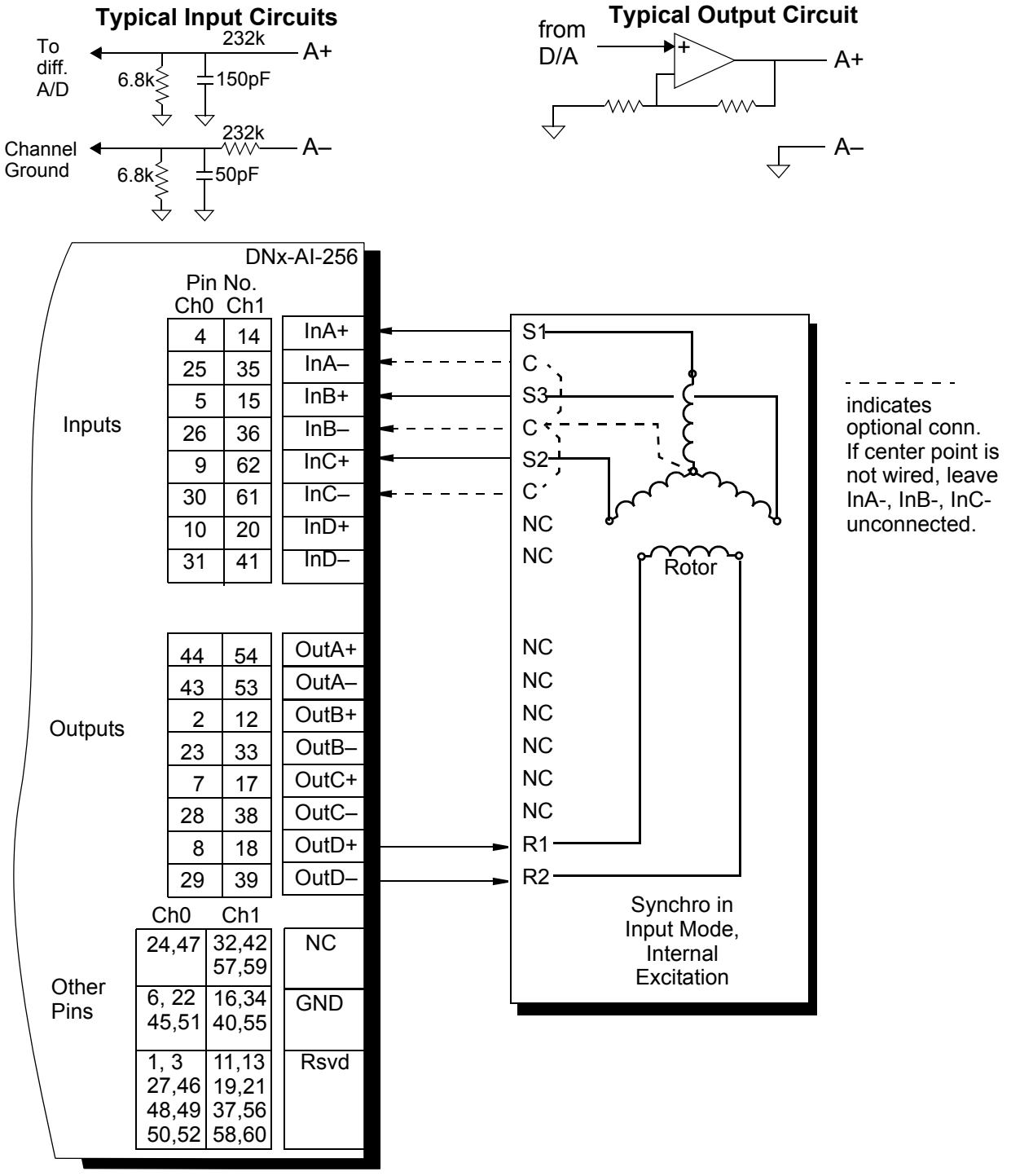


Figure B-1. AI-256 in Synchro Input Mode with Internal Excitation

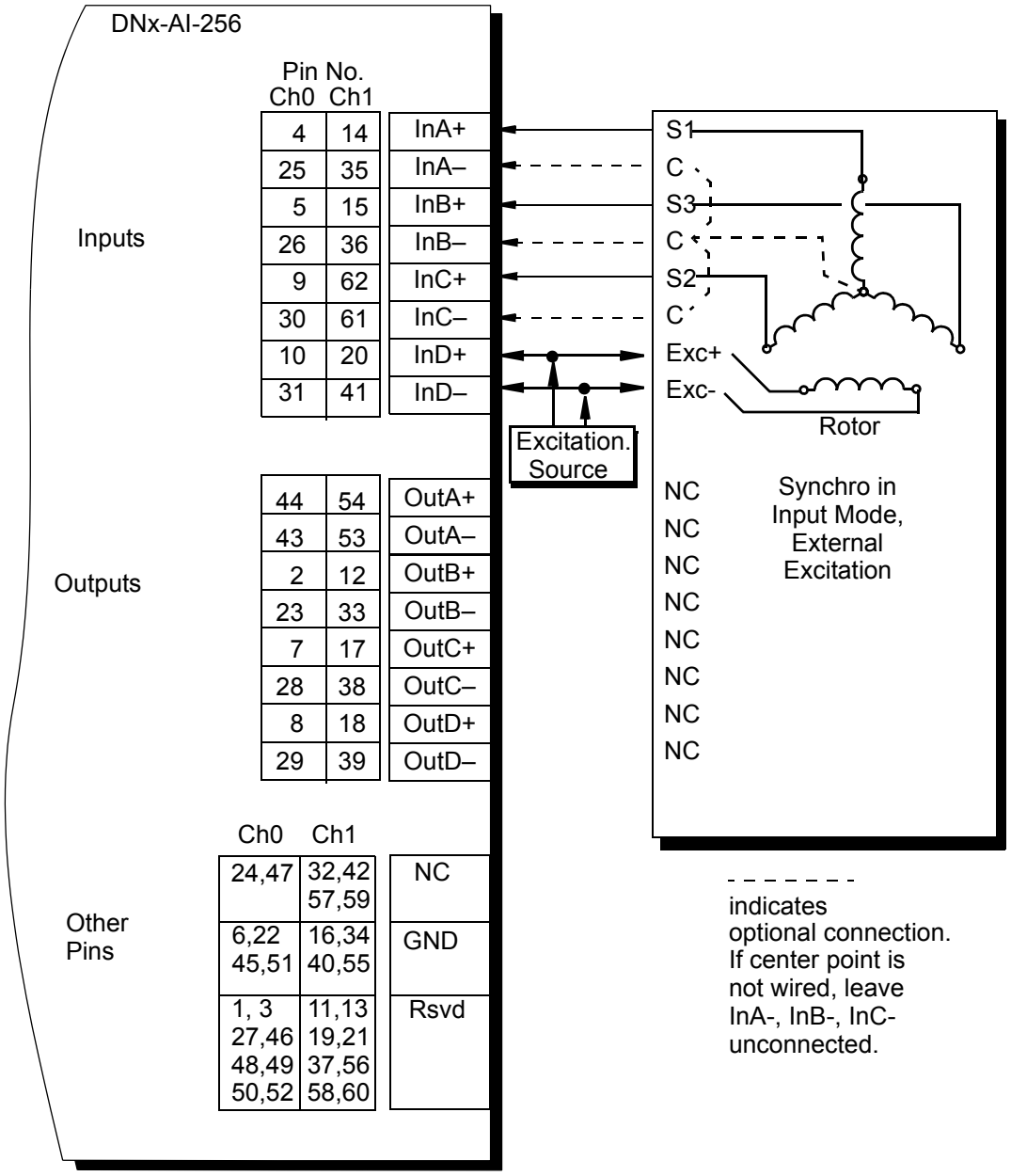
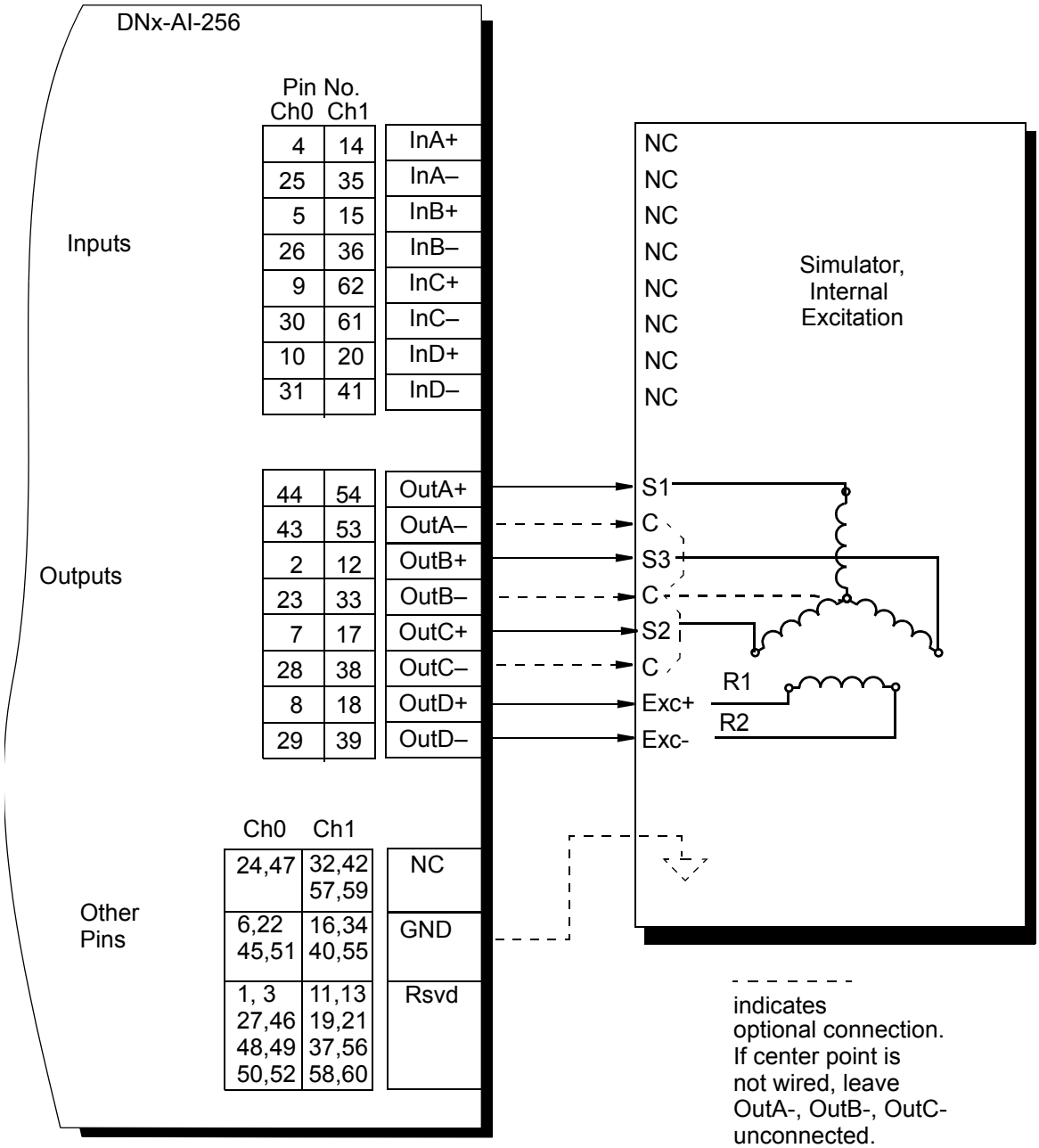


Figure B-2. AI-256 in Synchro Input Mode with External Excitation



NOTE: Most synchros do not require connections to OutA-, OutB-, and OutC-. Some devices, however, use electronic equivalents of synchros. In such cases, connect the channel ground to the device ground.

Figure B-3. AI-256 in Synchro Simulator Mode with Internal Excitation

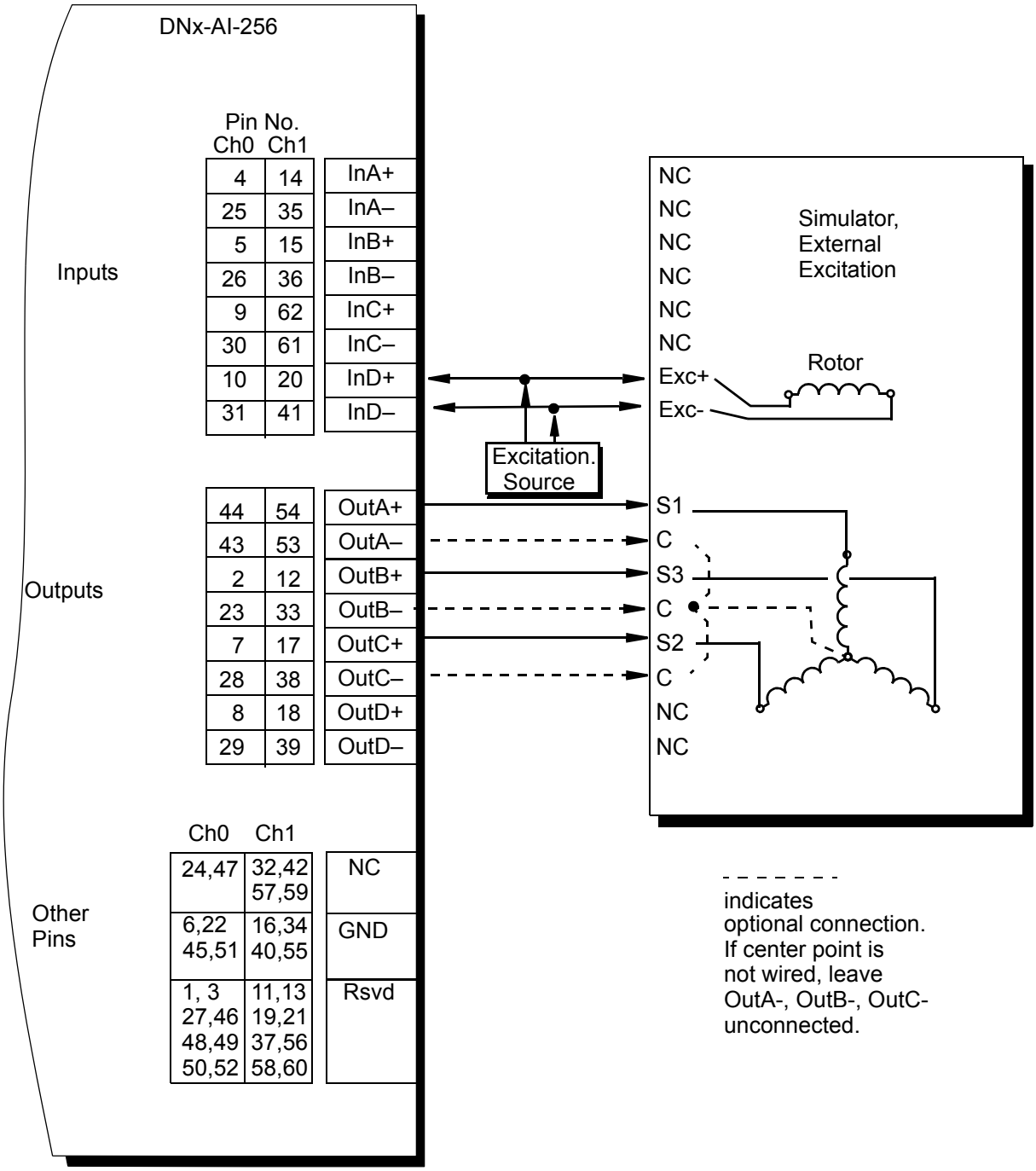
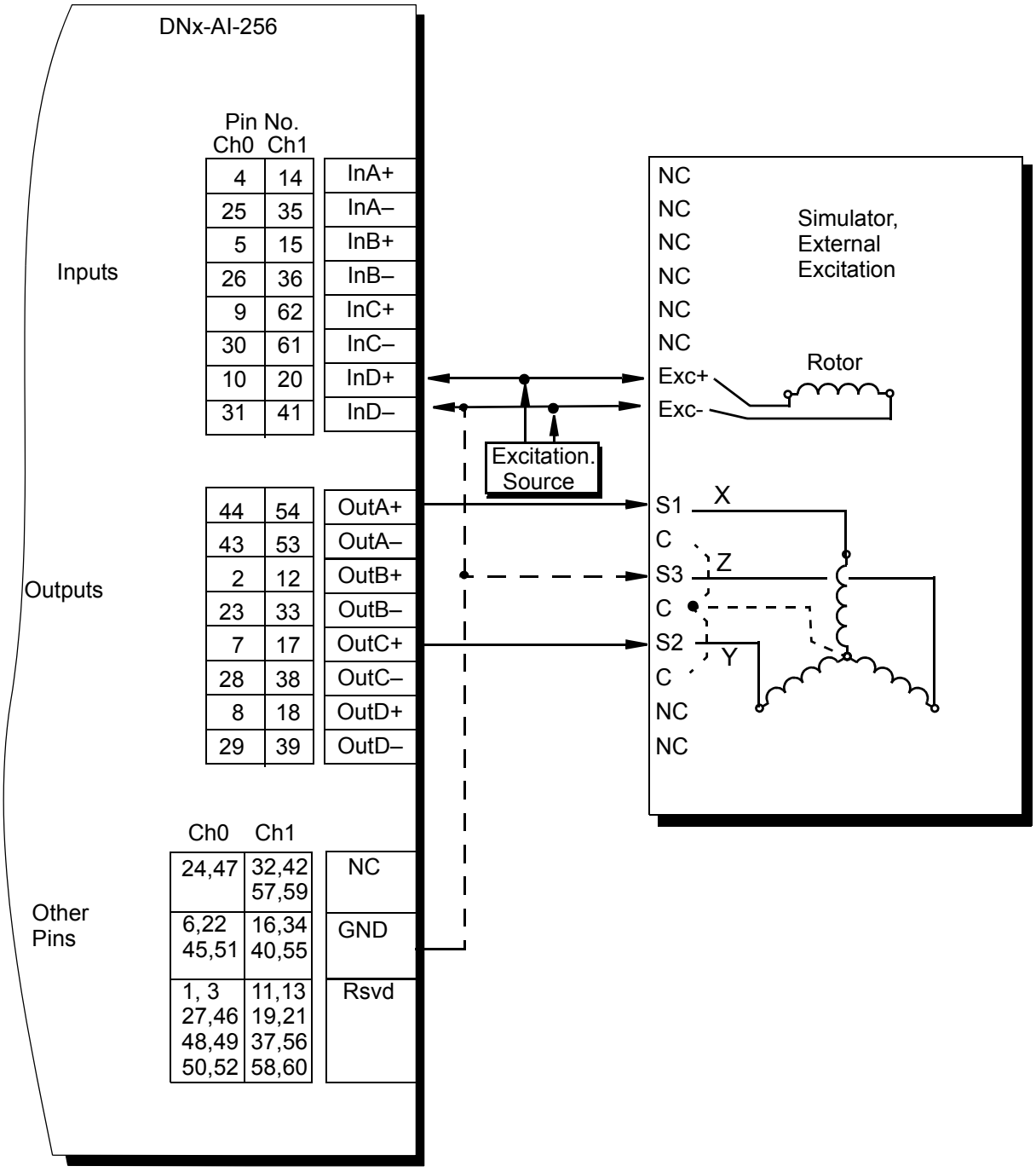


Figure B-4. AI-256 in Synchro Simulator Mode with External Excitation



AI-256 in Synchro Simulator Mode with External Excitation in Z-grounding Mode

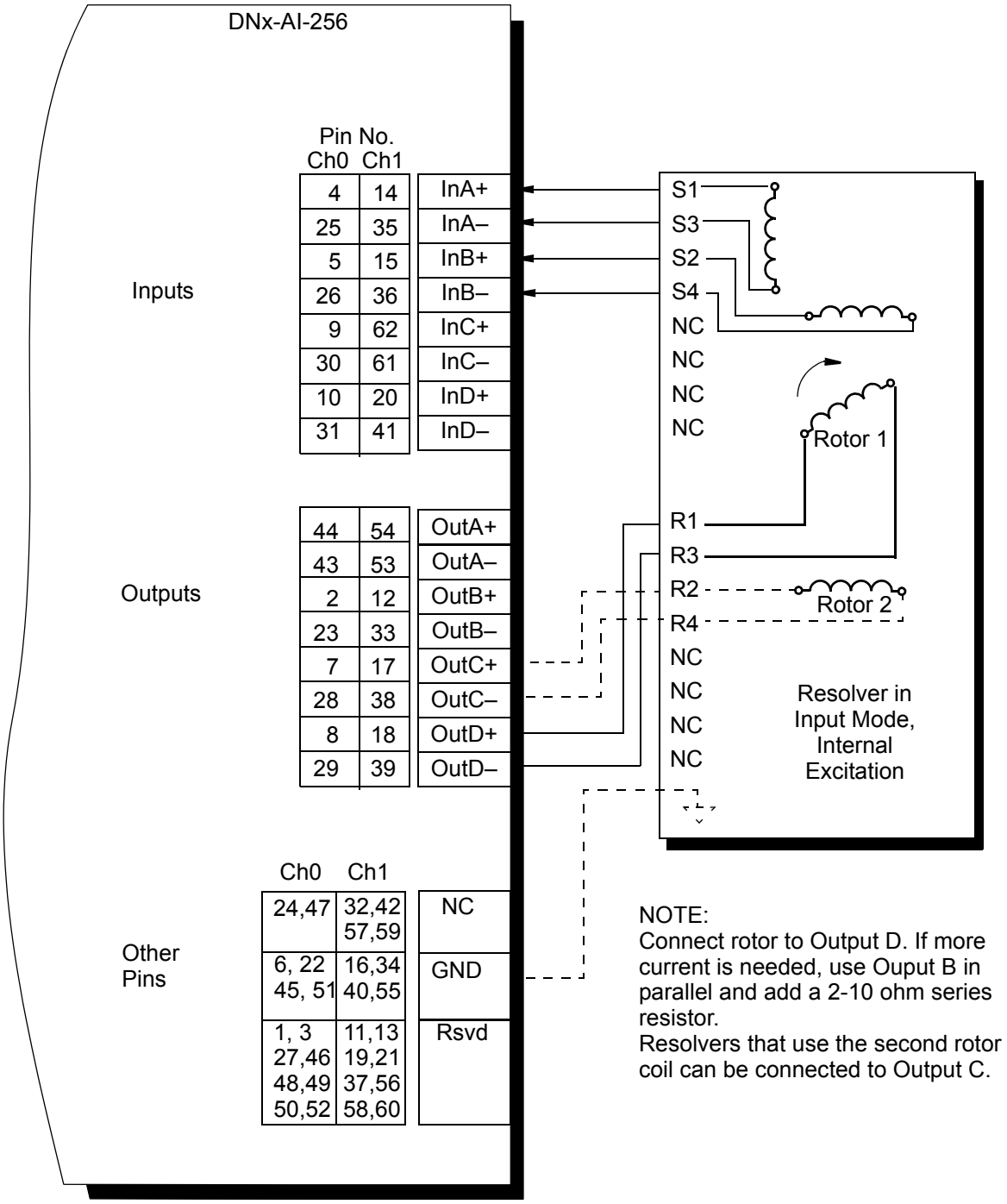


Figure B-5. AI-256 in Resolver Input Mode with Internal Excitation

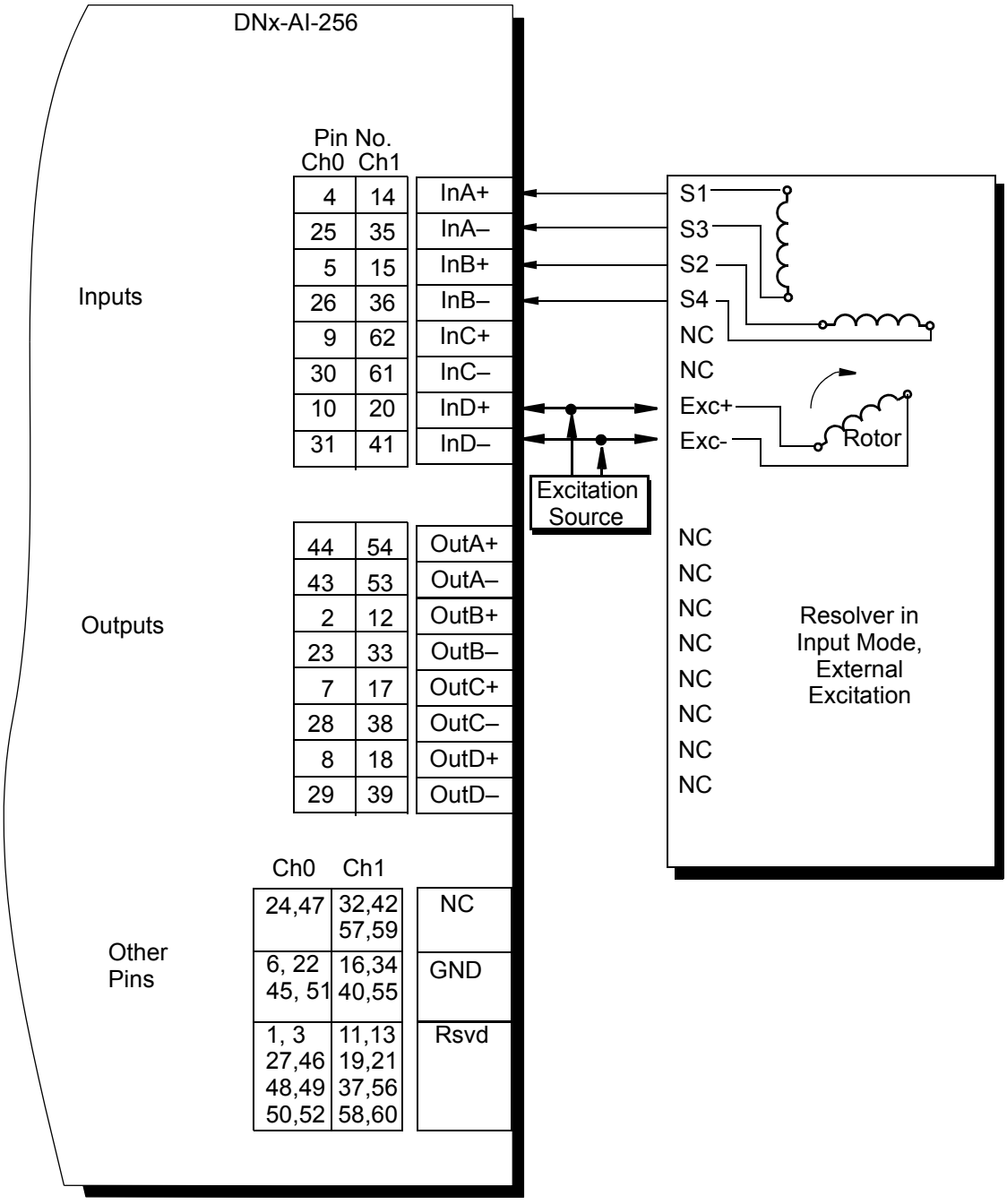


Figure B-6. AI-256 in Resolver Input Mode with External Excitation

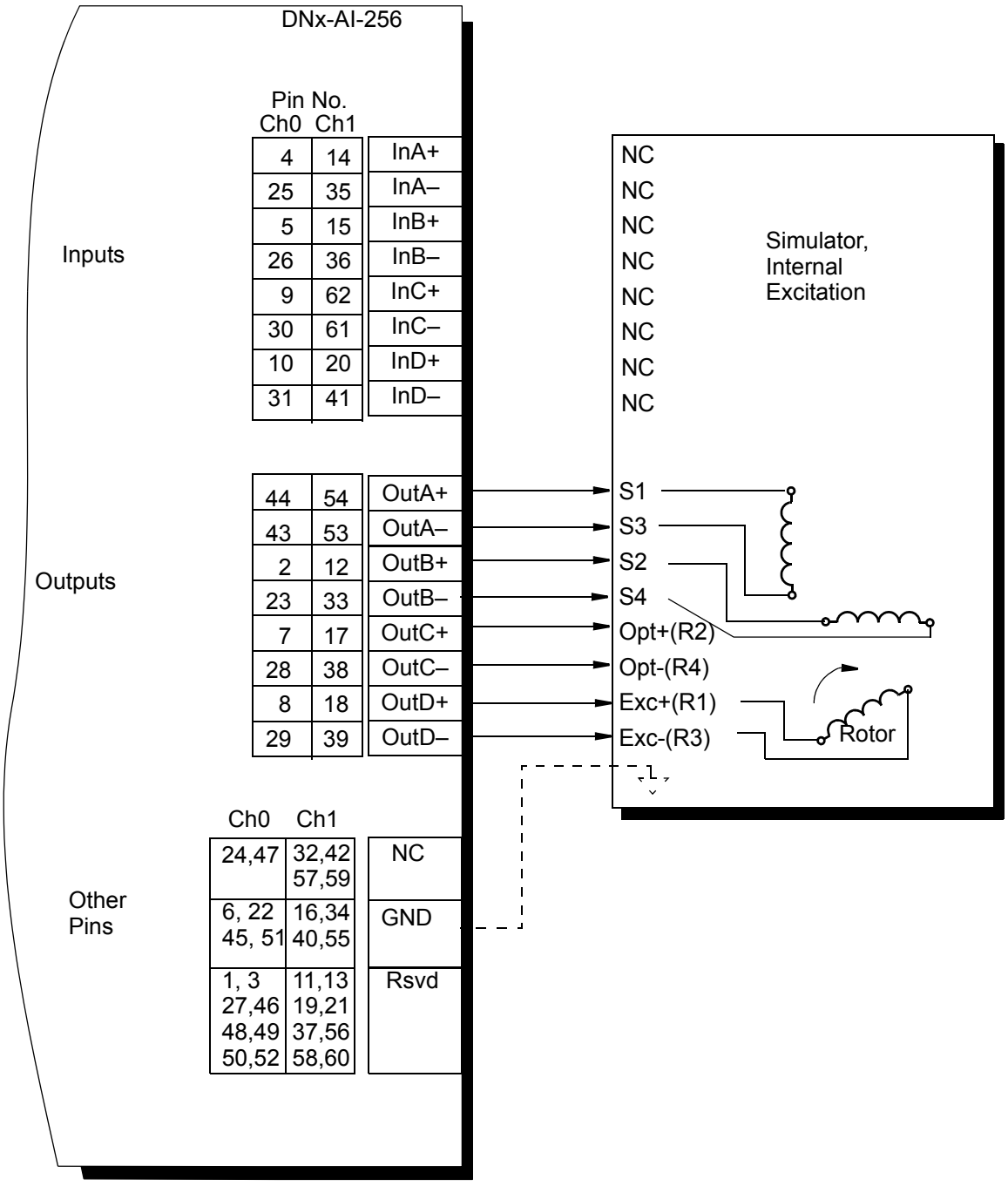


Figure B-7. AI-256 in Resolver Simulator Mode with Internal Excitation

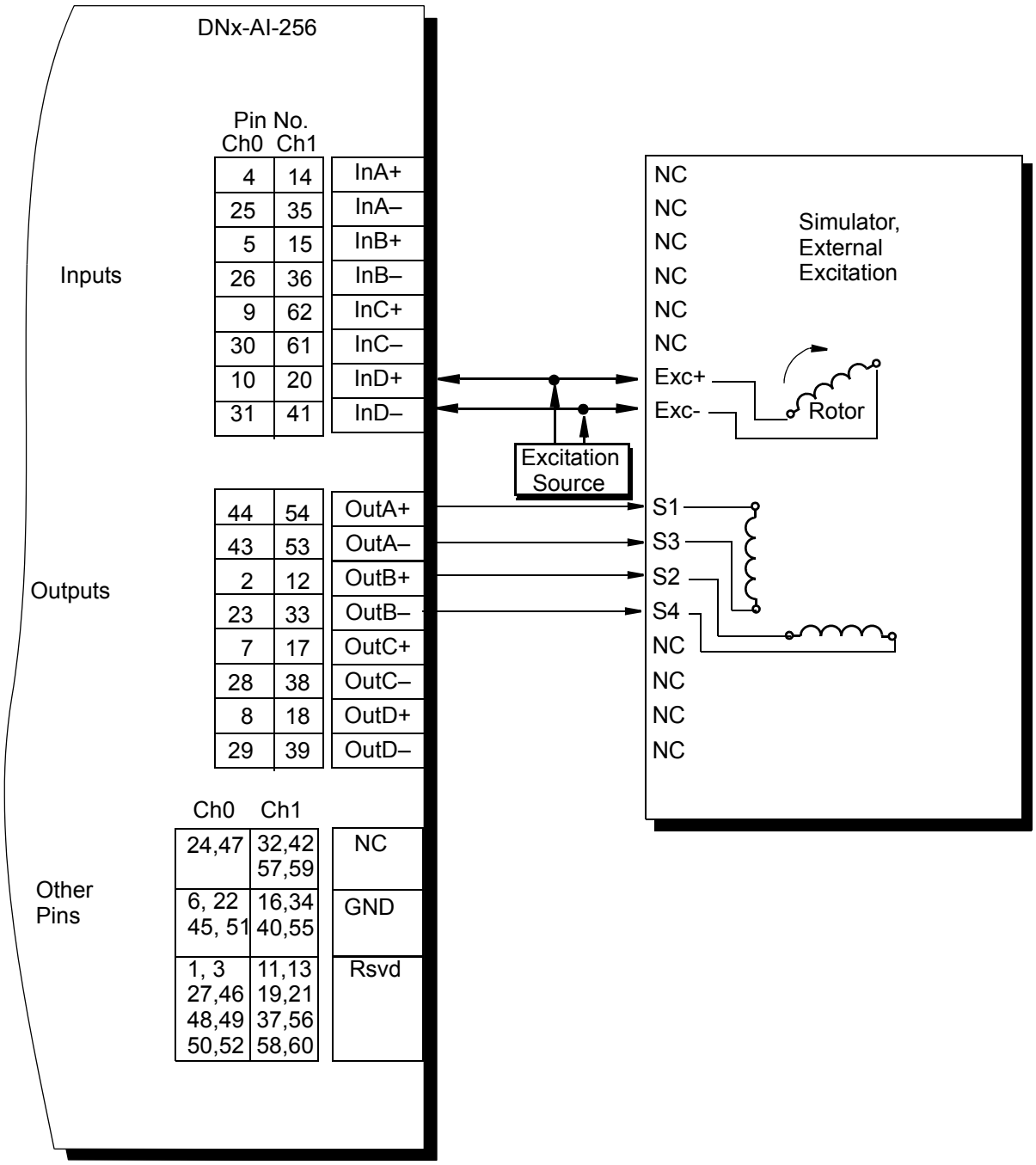


Figure B-8. AI-256 in Resolver Simulator Mode with External Excitation

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